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An Adaptable Interleaved DC-DC Boost Converter

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UNIVERSITY OF
PLYMOUTH

AN ADAPTABLE INTERLEAVED DC-DC BOOST CONVERTER

by

STUART MACVEIGH

A thesis submitted to the University of Plymouth in partial
fulfilment for the degree of

DOCTOR OF PHILOSOPHY

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0.2 Author's Declaration

At no time during the registration for the degree of Doctor of Philosophy has the author been registered for any other University award without prior agreement of the Doctoral College Quality Sub-Committee.

Work submitted for this research degree at the University of Plymouth has not formed part of any other degree either at the University of Plymouth or at another establishment.

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0.2.1 Publications

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STUART DAVID CHARLES MACVEIGH
AN ADAPTABLE INTERLEAVED DC-DC BOOST CONVERTER

Abstract

A.H. Weinberg presented his classic boost topology in his 1974 publication intended for use in satellites. It comprises minimal external components and uses multiple coupled coil systems to provide a boost of up to $2x$. Its simplicity makes it inherently robust and reliable as minimal components means lower chance of failure. While its simplicity makes it attractive it has limited boost capability which makes it unsuitable for many modern day applications. No significant investigation has been carried out on adapting the Weinberg topology for high boost operation so far as can be ascertained.

An investigation into adapting the Weinberg converter for high boost operation is presented in this thesis. A novel topology is developed which preserves the simplicity, reliability and efficiency of the Weinberg design while achieving boost ratios $>2x$. An analysis of the proposed topology is provided and mathematical expressions are derived to quantify the voltages and currents in relevant component for a given set of operating conditions. All coupled windings share a single core and are arranged so the magnetic flux does not reverse direction which further reduces loss in the magnetic core material. The coupled coils clamp the MOSFET drain voltage to an amount much lower than the output voltage which allows lower breakdown versions with lower intrinsic ON-resistance to be used leading to reduced conduction losses. Modelling of circuit losses and their sources allows optimal selection and positioning of components and finds wound component and MOSFET conduction losses contribute around 70% of the total circuit loss. Modelling and trialling of wound component geometries is carried out to optimise magnetic coupling and reduce leakage inductance.

Working prototypes are developed and used to verify the mathematical claims through experimentation. Overall system efficiency of 94.1% is achieved at a boost ratio of $8.8x$ and an output power of 257W. Overall system losses are reduced from 11% to 6% by simply optimising the magnetic assembly. However optimisation of the magnetic assembly is more involved and may be less tolerant to variation which may hinder repeatability but the results are very positive despite crude, hand-wound magnetic coils and standard quality silicon components being used; which is a promising sign.

Keywords: DC-DC Converter; Boost; Coupled Inductor; Interleaved; Weinberg; Efficiency; Reliability.

CONTENTS

0.1	Acknowledgements	1
0.2	Author's Declaration	2
0.2.1	Publications	2
1.	<i>Introduction</i>	14
1.0.1	Non-Isolated	16
1.0.2	Isolated	16
1.0.3	Literature Review	19
1.0.4	Topological Variations of the Conventional Boost Converter	21
1.0.5	Conventional Interleaved Boost Converters	22
1.0.6	Three-Level Boost Converters	24
1.0.7	Cascaded Boost Converters	26
1.0.8	Coupled-Inductor-Based Boost Converters	31
1.0.9	Switched-Capacitor-Based Boost Converters	41
1.0.10	Interleaved Boost Converters	48
1.0.11	Three-State Switching Cell (3SSC) Based Converters	55
1.0.12	The Weinberg Converter	65
2.	<i>Novel Adaptable Boost Converter</i>	69
2.0.1	Analysis of the Proposed Topology	71
2.0.2	Unregulated Output Voltage Analysis	71
2.0.3	Regulated Output Voltage Analysis	76
3.	<i>Prototype Experimentation</i>	94
3.0.1	Loss Analysis	97
3.0.2	Electrical Losses in Magnetic Windings	99
3.0.3	Magnetic Losses	108
3.0.4	Conduction Losses	116
3.0.5	Switching Losses	117
4.	<i>Discussion</i>	122
4.0.1	Modes of Operation	122
4.0.2	Prototyping	128

4.0.3	Applications	134
4.0.4	Maximum Power Point Tracking (MPPT) Applications with Constant Input and Output Voltages	135
4.0.5	How It Compares	136
5.	Conclusions	137
6.	Future Work	139
6.0.1	Analysis using Non-Ideal Components	139
	Bibliography	146
	Appendices	157
.1	Glossary of Terms and Abbreviations	158
.1.1	Acronyms	158
.1.2	Electrical Component Identifiers	158
.1.3	Electrical Mathematical Symbols	159
.1.4	Magnetics Mathematical Symbols	160
.1.5	General Mathematical Symbols	160
.2	LTSpice Simulation Schematics	161
.3	Control Circuit Schematic	164
.4	Magnetic core material characterisation	165
.5	Fourier Analysis of Inductor Currents	169
.6	Simulations for Non-Constant Output Voltage Operation	174
.7	Simulations for Constant Output Voltage Operation	181
.8	Non-constant output voltage prototype assembly	217

LIST OF FIGURES

1.1	Classic Boost Converter	18
1.2	Classification system of DC-DC Converters [24]	20
1.3	Conventional interleaved boost converter	22
1.4	A typical schematic for the three-level boost converter	24
1.5	Dual-switch quadratic boost converter	26
1.6	Single-switch quadratic boost converter	27
1.7	Multi-cascade single-switch DC-DC converter	27
1.8	Three-Level quadratic boost converter with reduced diodes [36] . . .	28
1.9	Conventional coupled inductor converter with voltage multiplier circuit [39]	29
1.10	Conventional coupled-inductor boost converter	31
1.11	A typical Flyback boost converter with clamp circuits	32
1.12	Flyback coupled-inductor boost converter	33
1.13	High output voltage Flyback topology [41]	35
1.14	Flyback converter combined with conventional interleaved topology [60]	36
1.15	Flyback converter combined with conventional interleaved topology and voltage multiplier cell [60]	37
1.16	Non-isolated Zero-Voltage Switched (ZVS) interleaved boost converter [61]	38
1.17	Interleaved converter with voltage multiplier stages [62]	39
1.18	Coupled inductor interleaved boost converter [63]	40
1.19	Switched capacitor boost converter	41
1.20	Proposed schematic for conventional boost topology incorporating switched capacitor technique [65]	43
1.21	Inverting and non-inverting switched-capacitor (SC) cell [66]	44
1.22	Proposed schematic for switched-capacitor based active network converter [30]	45
1.23	Adapted schematic for switched-capacitor based active network converter [30]	46
1.24	High step-up DC-DC converter using switched capacitor techniques [47]	47
1.25	Voltage Doubler Interleaved boost converter	48

1.26	Interleaved boost converter with voltage multiplier cells	49
1.27	Voltage doubling interleaved topology [70]	50
1.28	Improved voltage doubling interleaved topology [71, 72]	51
1.29	Modified interleaved AC-DC converter with Power Factor correction ability [78]	52
1.30	Multi-stage capacitor multiplier [73, 74]	53
1.31	Proposed WCCI topology [19]	54
1.32	Three-State-Switching-Cell (3SSC) boost converter	55
1.33	Three-State-Switching-Cell (3SSC) boost converter with Switched Capacitor (SC) voltage multiplier cells	56
1.34	3SSC based multiphase switching cell [25]	57
1.35	3SSC based coupled multiphase switching cell [25]	59
1.36	3SSC multiphase coupled [88]	60
1.37	3SSC based multiphase voltage multiplier using switched capacitors [83, 89, 90, 97]	62
1.38	3SSC based isolated bidirectional soft switching converter [85–87] .	63
1.39	Original Weinberg topology [1]	66
1.40	Classic Weinberg converter boost ratio vs turns ratio [1]	66
1.41	Weinberg further development topology [1, 2]	67
2.1	Proposed Topology	70
2.2	Mode 1: Both Switches Closed	73
2.3	Mode 2: One Switch Closed	74
2.4	Equivalent representation of the proposed topology	76
2.5	Current waveforms for all coils shown in Figure 2.4 using simulation data	77
2.6	Expanded input current waveform	78
2.7	Calculated vs simulated input current against switch-on time assuming complete dependence on switching	79
2.8	Expanded transformer current and voltage waveforms showing the node voltage V_N and primary coil current i_A over a switching period T	80
2.9	Equivalent circuit during overlap period $t_{(OV)}$	81
2.10	Equivalent circuit during output period $t_{(OP)}$ with S_1 open	83
2.11	Equivalent circuit during free-wheeling period $t_{(ID)}$	84
2.12	Expanded Output current Waveform	88
2.13	Output diode voltage waveforms over a switching period	91
3.1	Block diagram of prototype assembly	94
3.2	Current waveforms measured from final prototype assembly	96
3.3	Constant output voltage prototype assembly with microcontroller based switching control	97

3.4	Measured input (bottom) and output (top) power during prototype experimentation	98
3.5	Illustration of the Skin Effect in a single conductor	100
3.6	Illustration of the proximity effect on multiple conductor windings .	101
3.7	Plot of magnetic field strength in the magnetic cores over time using simulation data	109
3.8	Plot of magnetic field strength in the magnetic cores over time using real data	110
3.9	Plot of flux density in the magnetic cores over time using simulation data	112
3.10	Plot of flux density in the magnetic cores over time using real data	113
3.11	Magnetic flux density to power loss conversion chart for Sendust powder cores	114
3.12	Magnetic flux density to power loss conversion chart for Sendust powder cores	115
3.13	MOSFET voltage, current and power waveforms during switch-off .	118
3.14	MOSFET voltage, current and power waveforms during switch-on .	119
4.1	Simulated input current against switch-on time	123
4.2	Simulated boost ratio and input current against duty cycle when operating with an unregulated output voltage	125
4.3	Simulated boost ratio and input current against duty cycle when operating with a regulated output voltage	127
4.4	MOSFET drain voltage waveform against magnetic assembly build quality $V_{out} = 250V$	130
4.5	MOSFET Drain voltage waveforms when $V_{out} = 250V$	131
4.6	Constant output voltage final prototype assembly with STM-Discovery switching control board	132
4.7	Constant output voltage final prototype assembly power measurements	133
6.1	140
6.2	Ideal vs real diode responses using actual simulation data	142
6.3	Current waveforms for all coils using non-ideal components and simulation data	143
6.4	Expanded transformer current and voltage waveforms using non-ideal components	145
.5	LTSpice simulation schematic with ideal components and no losses .	162
.6	LTSpice simulation schematic with non-ideal components, losses and leakage inductances included	163
.7	Control circuit schematic with static dead time	164
.8	Magnetic core measurement assembly	166

.9	Sendust MS-106125-2 characterisation	167
.10	Sendust MS-157125-2 characterisation	168
.11	FFT of simulated current $i_{L_{in}}$	170
.12	FFT of simulated current i_{L_A}	171
.13	FFT of simulated current i_{L_B}	172
.14	Simulated vs calculated results for V_{out} while sweeping parameter L_{in} from $40\mu\text{H}$ to $400\mu\text{H}$	175
.15	Simulated vs calculated results for V_{out} while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$	176
.16	Simulated vs calculated results for V_{out} while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$	177
.17	Simulated vs calculated results for V_{out} while sweeping parameter V_{in} from 5V to 50V	178
.18	Simulated vs calculated results for V_{out} while sweeping parameter T from $1\mu\text{s}$ to $10\mu\text{s}$	179
.19	Simulated vs calculated results for V_{out} while sweeping parameter D from 0.1 to 0.9	180
.20	Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter L_{in} from $40\mu\text{H}$ to $400\mu\text{H}$	182
.21	Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter L_{in} from $40\mu\text{H}$ to $400\mu\text{H}$	183
.22	Simulated vs calculated results for Δi_{in} while sweeping parameter L_{in} from $40\mu\text{H}$ to $400\mu\text{H}$	184
.23	Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter L_{in} from $40\mu\text{H}$ to $400\mu\text{H}$	185
.24	Simulated vs calculated results for Δi_{out} while sweeping parameter L_{in} from $40\mu\text{H}$ to $400\mu\text{H}$	186
.25	Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$	187
.26	Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$	188
.27	Simulated vs calculated results for Δi_{in} while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$	189
.28	Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$	190
.29	Simulated vs calculated results for Δi_{out} while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$	191
.30	Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$	192

.31	Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$	193
.32	Simulated vs calculated results for Δi_{in} while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$	194
.33	Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$	195
.34	Simulated vs calculated results for Δi_{out} while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$	196
.35	Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter V_{in} from 5V to 50V	197
.36	Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter V_{in} from 5V to 50V	198
.37	Simulated vs calculated results for Δi_{in} while sweeping parameter V_{in} from 5V to 50V	199
.38	Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter V_{in} from 5V to 50V	200
.39	Simulated vs calculated results for Δi_{out} while sweeping parameter V_{in} from 5V to 50V	201
.40	Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter V_{out} from 100V to 1000V	202
.41	Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter V_{out} from 100V to 1000V	203
.42	Simulated vs calculated results for Δi_{in} while sweeping parameter V_{out} from 100V to 1000V	204
.43	Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter V_{out} from 100V to 1000V	205
.44	Simulated vs calculated results for Δi_{out} while sweeping parameter V_{out} from 100V to 1000V	206
.45	Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter T from $5\mu\text{s}$ to $50\mu\text{s}$	207
.46	Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter T from $5\mu\text{s}$ to $50\mu\text{s}$	208
.47	Simulated vs calculated results for Δi_{in} while sweeping parameter T from $5\mu\text{s}$ to $50\mu\text{s}$	209
.48	Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter T from $5\mu\text{s}$ to $50\mu\text{s}$	210
.49	Simulated vs calculated results for Δi_{out} while sweeping parameter T from $5\mu\text{s}$ to $50\mu\text{s}$	211
.50	Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter D from 0.1 to 0.9	212

.51	Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter D from 0.1 to 0.9	213
.52	Simulated vs calculated results for Δi_{in} while sweeping parameter D from 0.1 to 0.9	214
.53	Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter D from 0.1 to 0.9	215
.54	Simulated vs calculated results for Δi_{out} while sweeping parameter D from 0.1 to 0.9	216
.55	Non-constant output voltage prototype assembly	218
.56	Non-constant output voltage prototype assembly with power measurements	219
.57	Non-constant output voltage prototype assembly fitted for testing	221
.58	300W solar panel in position used for testing	222
.59	Non-constant output voltage prototype assembly power measurements from testing	223

LIST OF TABLES

3.1	Properties of the MicroMetals T184-26 iron powder core	103
3.2	Properties of the MS-157125-2 Sendust powder core	104
3.3	AC resistance values over N_h harmonics	105
3.4	Parameters involved in eddy current loss analysis from [101]	107
4.1	Constant output voltage final prototype assembly component list . .	132
.1	Magnetic winding current magnitudes over N_h harmonics	173
.2	Non-constant output voltage prototype assembly component list . .	220

Various acronyms and abbreviations are used throughout this thesis. Please refer to Appendix .1 for definitions.

1. INTRODUCTION

A.H. Weinberg in his 1974 publication [1] proposed a boost converter topology that does not seem to have been rigorously investigated.. Some adaptations exist [2–9] and an application using Weinberg’s proposed topology is presented in [10] but no analysis seems to have been carried out.

In this thesis Weinberg’s topology is adapted for high-boost applications and a full analysis is performed.

Section 1 provides an overview of the evolution of DC-DC converters over recent decades. Section 2 introduces the novel topology and presents the analysis including relevant mathematical derivations and identifying and quantifying sources of power loss. Section 3 covers the build of a real-world prototype and its use to verify the analytical claims. Section 4 discusses the merits of the novel topology in comparison with other notable designs from recent years.

Applications of DC-DC converters have become abundant in modern renewable energy systems. Such systems produce variable outputs as they are dependent on unregulated naturally occurring phenomena. The intensity of the sun, strength of the wind and tides are all subject to long and short term variability; ranging from seconds to hours. These systems are being tied to a regulated entity (the electrical grid) and need to be able to take these unpredictable variations and self-adjust their operation to satisfy these requirements. DC-DC converters are an ideal solution for this as they have the ability to do just that with high efficiency.

Existing domestic Photo-Voltaic (PV) systems use a string of series connected PV cells each of which generates around 36–45VDC reaching around 360VDC or 200VDC total in the UK and USA respectively. Little to no DC-DC conversion is needed here, a phase-aligned inverter is used to simply convert to AC and inject the power into the mains grid at 230Vrms or 120Vrms in the UK and USA respectively.

While this configuration allows for minimal power conversion and hence lower losses, series connected PV cells suffer from ‘shading’ issues [11–17]. Partial shading on any of the individual panels significantly degrades the performance of the entire string. Mismatching of the modules also reduces the overall performance as the weakest module will restrain the performance of the others. For example, if a string of series-connected PV cells consists of seven 8-amp cells and one 4-amp cell then the entire string is limited to 4 amps. In light of such drawbacks it is more efficient to use a parallel configuration [18]. However, problems with parallel

connected PV arrays include significant shortening of the PV cell lifespan [19]

Since none of the panels will have exactly the same voltage, the panel with highest voltage in the array will do a great majority of the work. Only when the first panel saturates and its voltage falls will the second highest voltage panel begin to contribute and so on.

For residential PV arrays, where cost is an important factor, non-isolated DC-DC converters have become the usual option [20, 21]. One factor in PV cell arrays is the reduction and management of leakage currents and topologies have been suggested to deal with this [22]. In order to reduce losses other designs tend to avoid basic topologies because of the high duty cycles required to obtain high boost ratios [23].

Power conversion efficiencies in excess of 90% are typically achieved for modern day topologies, therefore these circuits are designed to avoid high voltage stresses and excessive component count [19].

DC-DC converters serve two main purposes

1. Conversion

If a load is supplied from a stabilised DC supply but requires a voltage higher or lower than that being supplied it is necessary to ‘convert’ that voltage to suit. This can be done using a fixed ratio (operating at a fixed duty cycle) converter .

2. Regulation

Many modern day loads require regulated supplies. For applications such as digital, logic or amplifier circuits only the voltage needs to be regulated. Alternatively the current can be regulated for applications such as LED driving.

If feedback control is employed in a DC-DC converter it can then serve the purpose of a DC voltage regulator. By feeding back aspects of the converter’s operation to the switch controller such as the output voltage, output current, switching current etc. the controller can then adjust the switching characteristics of the converter to keep the output voltage or current at a static or ‘regulated’ value. This now allows DC-DC converters to take the place of the old fashioned Linear Regulators in high power applications.

DC-DC power converters use magnetic principles to step-up or step-down one DC voltage to another DC voltage via a high frequency switched inductor. There are two main types

- Boost: for stepping up

- Buck: for stepping down

of these there are also two main sub-types.

1.0.1 Non-Isolated

The basic Boost and Buck circuits are non-isolated as their inputs and outputs are not electrically separated. There is a single inductor which electrically connects the input to the output in both of these topologies. If the switching developed a fault (failed open for boost or failed short for buck) the inductor would behave like a short circuit and the supply voltage would pass through to the output. In the case of step-down topologies this could allow potentially harmful voltages to appear at the output where they may do damage to sensitive and/or expensive equipment or even come into direct contact with people or animals.

1.0.2 Isolated

In isolated topologies a transformer arrangement is used where the switched inductor has more than one winding around a common core. The primary (or driving) coil is connected to the supply and switched at high frequency with a MOSFET switch to provide excitation to the magnetic system and builds energy within it. The secondary (or driven) coil is connected to the output and exports the energy out of the magnetic system to the load. There is no direct electrical connection between the input and output so isolated topologies are safer for appliances which require connection to the electrical supply and come into direct contact with people such as mobile phone chargers and consumer electronics. In previous years this would have been achieved by simply using an isolating transformer followed by a linear voltage regulator or basic step-down converter. Isolating transformers for use at the electrical utility frequencies (50-60Hz) are big and heavy because a large volume of magnetic material is required to prevent saturation at such low frequencies. Modern designs strive to reduce product size and weight. They rectify the high voltage input to DC first then drop it to a low voltage through an isolated DC-DC converter circuit allowing the use of a much smaller transformer.

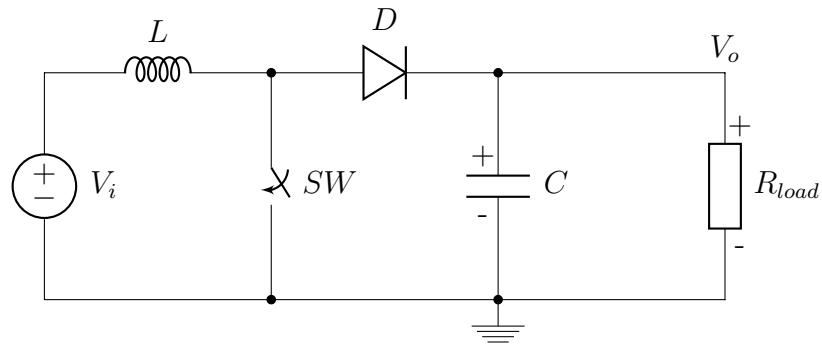
In ‘Forward’ Converters energy is passed through the transformer using magnetic coupling. In ‘Flyback’ Converters the output is blocked by a reverse diode while the switch is closed so energy is stored in the transformer core. The diode conducts when the switch opens and the energy is passed to the output.

Difficulties with many non-isolated Flyback converters, especially the classic topology, include efficiency loss at high boost ratios. Classic boost topologies cannot operate efficiently above boost ratios of about 4x [24]. At ratios much in excess of this, classic boost topologies also suffer from voltage ripple and instability on the output due to the high duty cycles. Large duty cycles are required to

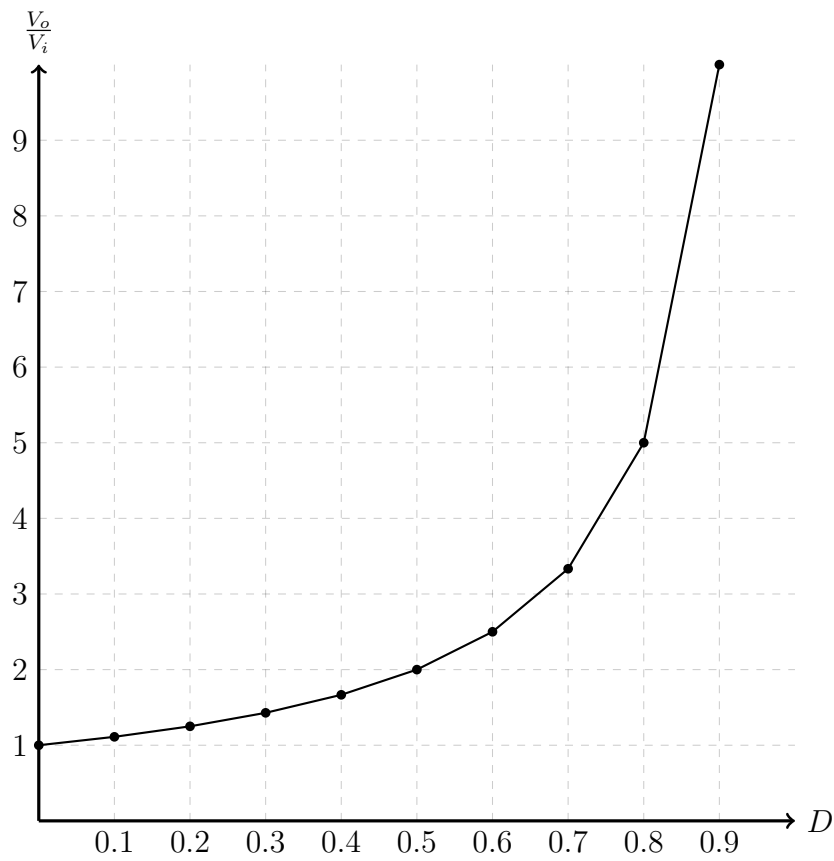
produce high boost ratios. Under these conditions tiny changes in duty cycle produce large effects on the output leading to control difficulties and instability [25].

The classic boost topology is shown in Figure 1.1. The transfer function plot shows how a small change in duty cycle creates an increasing change in boost ratio as the duty cycle rises. If the duty cycle is adjusted from 10% to 11% the boost ratio changes by 0.012. If the duty cycle is adjusted from 80% to 81% the boost ratio changes by 0.26; a 20x larger effect. This could translate to an output voltage swing of several volts in high boost applications which results in high output voltage ripple.

Topologies have evolved to include coupled inductors and transformer arrangements to allow equivalent boost ratios to be achieved using much lower duty cycles which greatly increases controllability and stability. The use of coupled inductors has also been applied to provide magnetic energy paths for storage inductors to alleviate switching spikes.



(a) Topology



(b) Transfer Function plot

$$\frac{V_o}{V_i} = \frac{1}{1-D}$$

Fig. 1.1: Classic Boost Converter

1.0.3 Literature Review

Developments in space applications in the 1960s resulted in an increased focus on renewable energy sources which gave rise to the requirement for more efficient and stable power conversion. Renewable sources produce low voltage unregulated outputs and are used to supply loads, most of which require stabilised power input and sometimes at much higher voltages. Renewable energy is limited so efficiency is important and operation is often in remote locations, such as satellites, so reliability is also key. This section reviews the evolution of step-up (boost) DC-DC converters over the last fifty years, since they garnered increased interest in the 1970s.

Slobodan Ćuk [26] was amongst the first to develop a boost/buck combined converter with works going back to the mid 1970's and allowing for conversion over larger input and output voltage ranges. Ćuk further developed his work over the following fifteen years with the help of others such as D. Maksimovic [27] who produced a quadratic topology where the voltage gain is proportional to the square of the duty cycle. By modern standards the efficiency is relatively low at around 83%. These fall well short of modern expectations, but they did show the benefits of reducing circuit complexity to reduce losses within the system.

An overview of many recent DC-DC converter topologies is provided in [24,28]. It includes reviews of a selection of Non-isolated DC-DC boost converters and proposes a classification system that attempts to group the various topologies so they can be more easily compared against each other (Figure 1.2). Examples of literature from each group are compared and their strengths and weaknesses are highlighted. This review uses the layout in Figure 1.2 as a guide to determine the similarities between the work contained in this thesis to that of current designs and theories.

As higher boost systems meet more of the increasing demands, there have been several different attempts made to devise the optimal topology.

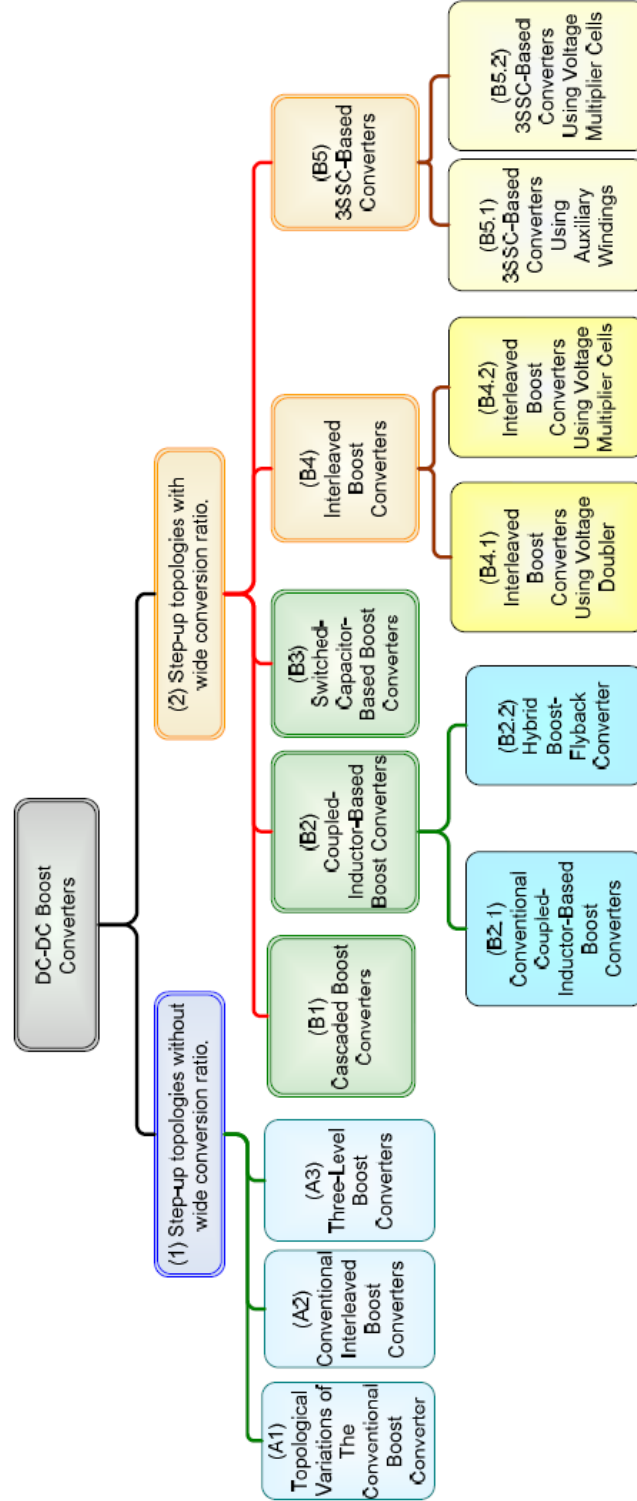


Fig. 1.2: Classification system of DC-DC Converters [24]

1.0.4 Topological Variations of the Conventional Boost Converter

The conventional boost converter is theoretically attractive due to its simple design but has limitations. It uses the concept of voltage boosting by switched inductor at its most basic. It is composed of a single inductor and active switching element which are subjected to all current and voltage stresses of the power transfer. This has great influence on the converter cost, performance, and efficiency [29].

It is acknowledged that the conventional boost converter has the benefit of being simple in structure and has uses in Power Factor correction applications [28]. Here voltage boosting is not the primary application, therefore high duty cycles are not required and the circuit can be allowed to operate within its most efficient region. Converters where the boost ratio is purely dependent on the duty cycle are undesirable. While high boost ratios can be achieved, it requires high duty cycles which subject the switching component(s) to large voltages and currents which causing stress which can consequently lead to shortened component lifespan and premature failure. In order to maintain efficiency and performance within systems it is imperative that these stresses are minimised otherwise a high cost is incurred in creating a solution [30].

The boost ratio tends towards infinity as the duty cycle tends to unity [24,31]. At very high duty cycles the stresses on the components become untenable and the efficiency drops as a consequence [28].

1.0.5 Conventional Interleaved Boost Converters

The conventional interleaved boost topology is shown in Figure 1.3. This topology has the same boosting characteristics as the conventional boost converter but is intended for very high current applications. Excessively high duty cycles, and associated complications, will still be required to achieve large boost ratios. In this sense the conventional interleaved topology has no benefit over the conventional converter. This topology is intended for applications where high current delivery is required but with only a small voltage boosting. Here all the main power components are duplicated in parallel to allow multiple current paths. The large current can then be split down multiple paths and alleviate the stresses on the components as each set are only subjected to a fraction of the overall current.

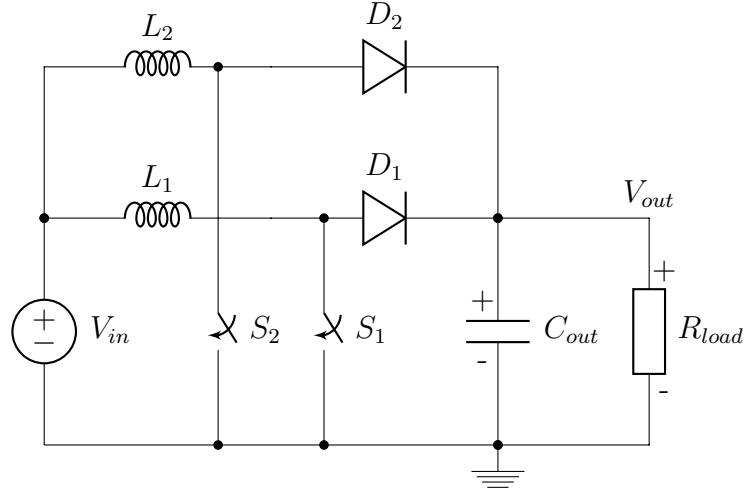


Fig. 1.3: Conventional interleaved boost converter

Each path consists of its own inductor, switch, and diode. The switching can be offset in time, or ‘Interleaved’, to produce a more continuous current throughput. Switching all at once results in large current surges. Interleaving increases the effective operating frequency and reduces the current ripple. If multiple paths are offset equally in time then the effective operating frequency will be multiplied up by the number of parallel paths available.

In Figure 1.3 switch S_1 closes and charges inductor L_1 . When S_1 opens L_1 discharges through diode D_1 and supplies the load. Capacitor C_{out} smooths the ripple generated by the switching to satisfy the load. S_2 , L_2 , and D_2 perform the exact same operation but are delayed in time by half a switching period $\frac{T}{2}$. There are now two systems feeding to the output in the same time period so the effective operating frequency is doubled. If both switches were closed and opened together the switching frequency would remain the same. The current ripple would also

worsen.

Work involving this topology has been presented in [32] which uses overlapped switching to switch each of the parallel transformer arrangements alternately. It also includes an ‘auxiliary’ circuit to reduce the switch stresses by allowing them all to turn on and off under Zero-Current Switching (ZCS) conditions but adds complexity to hardware and control timings. Efficiency loss may also occur as a portion of the input energy is used to power the oscillation in the auxiliary circuit. There was only a narrow power range of interest and results are restricted to that range.

1.0.6 Three-Level Boost Converters

The three-level boost converter is shown in Figure 1.4 and is designed to alleviate voltage stresses rather than current stresses [33]. The power components are doubled up in series meaning each one is only subjected to a proportion of the output voltage rather than all of it; as is the case with the basic topology. This allows lower breakdown voltage MOSFETs with lower ‘on-resistance’ to be used which reduces losses and increases efficiency.

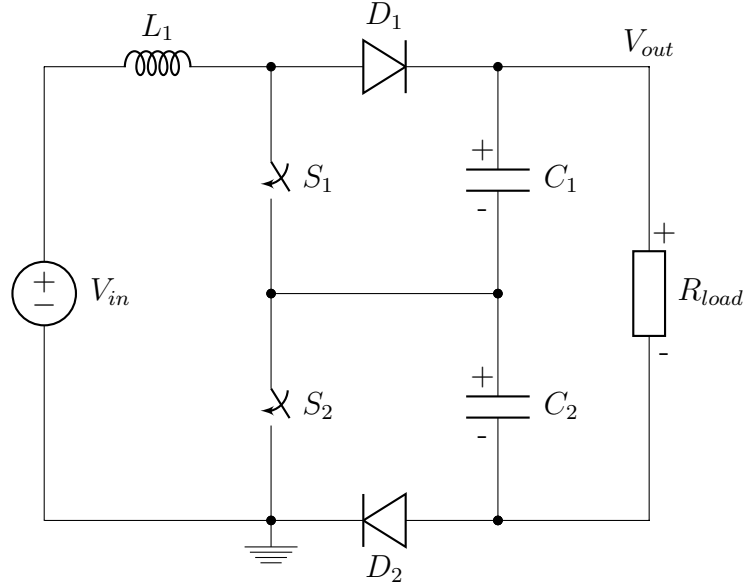


Fig. 1.4: A typical schematic for the three-level boost converter

The three-level converter can produce double the voltage gain of the conventional converter without subjecting the switching components to any additional voltage stresses.

In Figure 1.4 switches S_1 and S_2 have an equal duty cycle of D_S offset in phase by 180° . They close together which charges inductor L_1 . Then S_2 opens so L_1 discharges into capacitor C_2 . C_2 is charged to $V_{in} \frac{1}{1-D_S}$. S_2 closes again to recharge L_1 . Diode D_2 prevents C_2 from discharging during this phase. When L_1 is recharged S_1 opens so L_1 discharges into C_1 through diode D_1 . D_1 also prevents C_1 from discharging while S_1 is closed. Both capacitors are now charged to voltages given by $V_{in} \frac{1}{1-D_S}$ giving a total output voltage of $2V_{in} \frac{1}{1-D_S}$, assuming $D_{S_1} = D_{S_2}$.

The maximum voltage boost that can be produced by the conventional converter while maintaining acceptable efficiency and stability is around 4x. The three-level converter increases this limit to around 8x.

Work involving this topology has been presented in [33–35].

A three-level boost topology was presented in [33]. It follows the basic topology (Figure 1.4) and makes comparisons against the conventional converter. In this design the switches are interleaved in order to charge the output capacitors in turn. It is stated that when the input voltage is less than half the output voltage, which constitutes high gain conditions, the voltage across the components is halved. Also that through nature of its operation the three-level boost topology has a quarter of the inductor current ripple as the conventional converter hence the inductance can be quartered reducing conduction losses. The robustness, size and cost of the design will benefit from this.

[34, 35] also follow the basic topology (Figure 1.4). An AC voltage source is positioned at the centre-point of the circuit allowing the converter to behave as an AC-DC converter with the intention of performing power-factor pre-regulation.

1.0.7 Cascaded Boost Converters

When the required boost ratio is higher than around 8x a single converter stage based on the conventional topology will no longer suffice. A typical cascaded boost converter is shown in Figure 1.5. It is comprised of two conventional converter topologies cascaded together which has the effect of multiplying their transfer functions which produces

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1-D)^2}$$

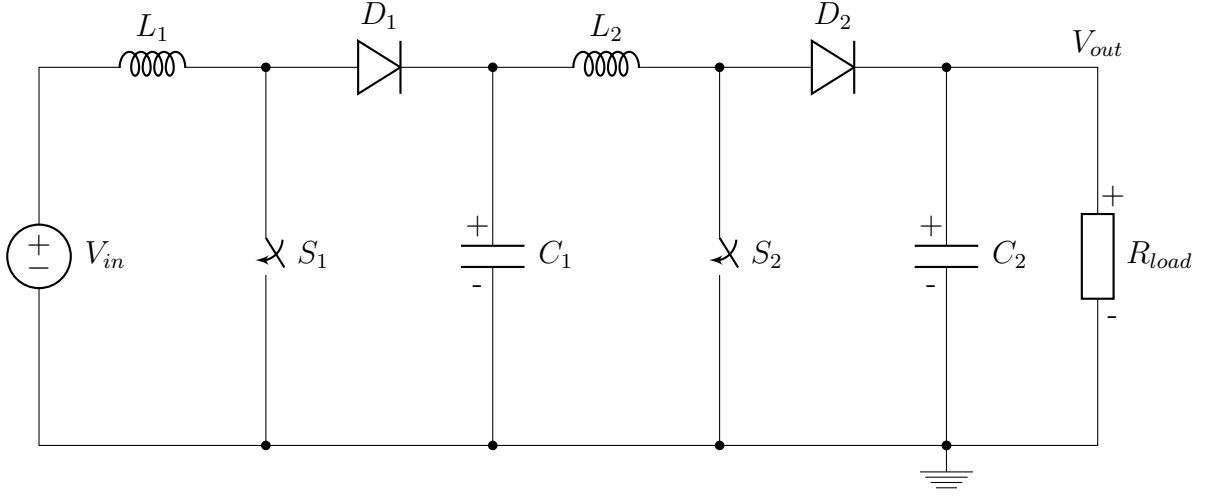


Fig. 1.5: Dual-switch quadratic boost converter

In Figure 1.5 switches S_1 and S_2 can be controlled together or independently as the two stages do not interfere with each other. The two-stage version shown in Figure 1.5 is better known as the Quadratic converter. One of the switches can also be replaced by a diode to allow a single switch to control the whole converter as shown in Figure 1.6. This reduces the switching component count and allows for simpler control.

In Figure 1.6 switch S_1 closes and charges inductor L_1 through diode D_3 . When S_1 opens L_1 discharges through diode D_1 and capacitor C_1 is charged to a voltage of $V_{C_1} = V_{in} \frac{1}{1-D}$. When S_1 closes the next time L_1 is recharged through D_3 . L_2 is also charged from C_1 . When S_1 opens L_1 discharges through D_1 and C_1 is charged to a voltage of $V_{C_1} = V_{in} \frac{1}{1-D}$. L_2 discharges through D_2 and C_2 is charged to a voltage of $V_{out} = V_{C_2} = V_{C_1} \frac{1}{1-D}$. This gives an overall transfer function of

$$V_{out} = V_{in} \frac{1}{(1-D)^2}$$

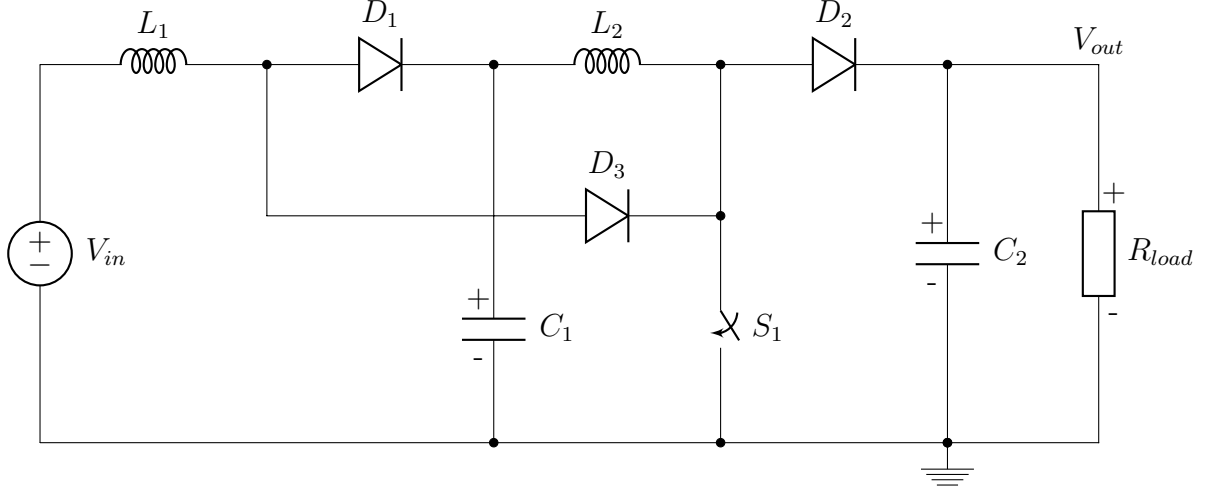


Fig. 1.6: Single-switch quadratic boost converter

Many stages can be cascaded together. Theoretically cascading N conventional boost converters should produce a transfer function of

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1 - D)^N}$$

Multiple cascaded stages can also be controlled with a single switch as shown in Figure 1.7. Each stage individually has a low boost ratio but the total boost over the cascade is much higher.

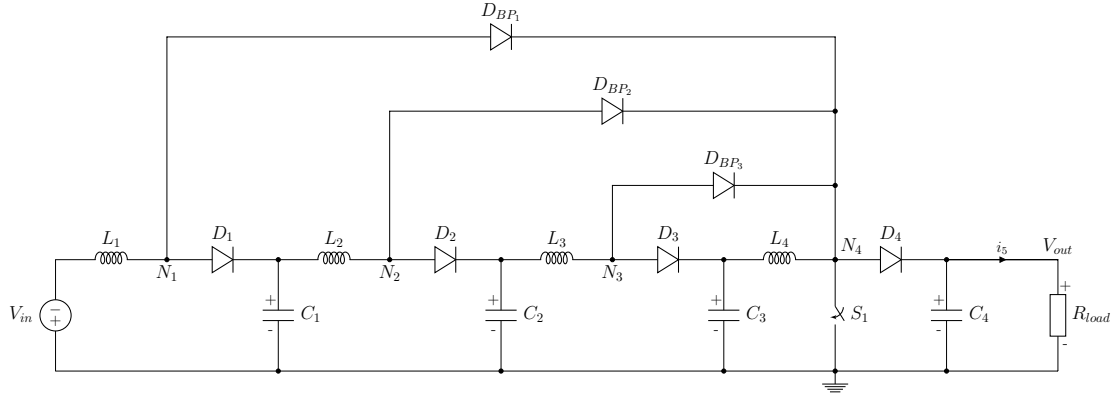


Fig. 1.7: Multi-cascade single-switch DC-DC converter

In Figure 1.7 switch S_1 closes and pulls nodes N_1, N_2, N_3, N_4 to ground. This allows inductors L_1, L_2, L_3, L_4 to charge through diodes $D_{BP1}, D_{BP2}, D_{BP3}$ respectively. Diodes D_1, D_2, D_3, D_4 block to prevent capacitors C_1, C_2, C_3, C_4 from discharging

during this period. When S_1 opens L_1, L_2, L_3, L_4 discharge through diodes D_1, D_2, D_3, D_4 respectively to recharge the capacitors. N_4 is at the highest potential so diodes $D_{BP1}, D_{BP2}, D_{BP3}$ block to prevent back-currents. Essentially each stage behaves like an individual conventional converter. In Figure 1.7 there are four stages so the ideal transfer function would be

$$V_{out} = \frac{1}{(1-D)^4} V_{in}$$

The quadratic topology can also be merged with the three-level topology (Figure 1.8) as proposed in [36].

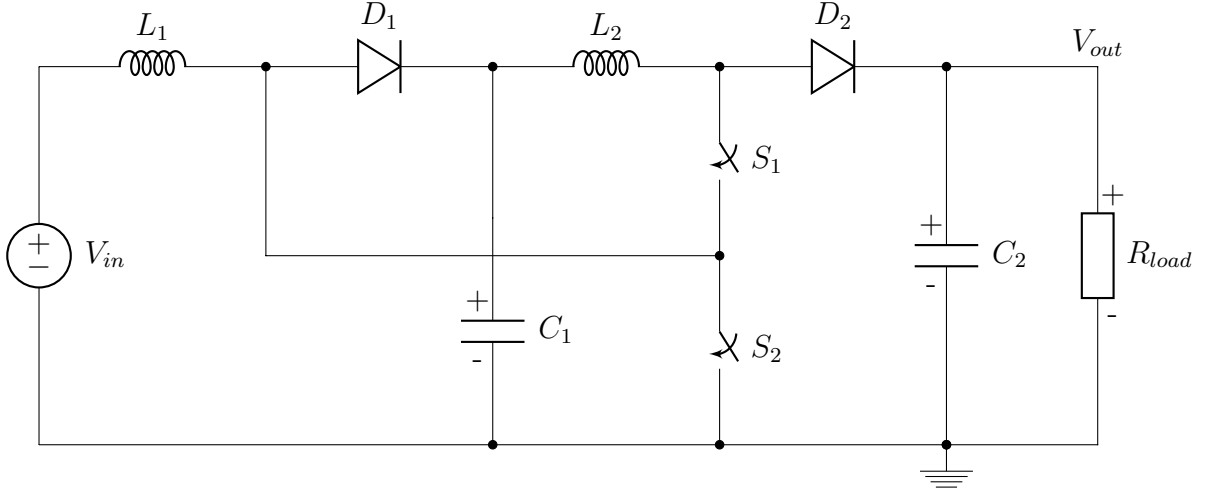


Fig. 1.8: Three-Level quadratic boost converter with reduced diodes [36]

In Figure 1.8 assuming steady-state operation capacitor C_1 will have a voltage of $V_{C1} = V_{in} \frac{1}{1-D}$. Switches S_1, S_2 close together. Inductor L_1 charges from the supply by passing current through S_2 . Inductor L_2 charges from C_1 by passing current through both S_1 and S_2 . S_1 opens first and inductor L_2 discharges through diode D_2 and charges C_2 to a voltage of $V_{out} = V_{C2} = V_{C1} \frac{1}{1-D}$. This takes charge out of C_1 causing its voltage to drop. When S_2 opens a short time later L_1 discharges through diode D_1 and recharges C_1 to a voltage of $V_{C1} = V_{in} \frac{1}{1-D}$. The overall transfer function is

$$V_{out} = \frac{1}{(1-D)^2} V_{in}$$

A quadratic three-level boost converter (as shown in Figure 1.8) is proposed in [36]. This topology is in essence two cascaded conventional boost converters but the voltage across the switches is halved due to their series connection. Merging the cascade with the Three-Level switching topology allows for greater boost while including the benefits of component voltage stress reduction.

A two-stage cascaded converter is proposed in [37] which claims to achieve a 3.5x higher boost ratio than the conventional converter at 50% duty cycle with an efficiency around 90%. However this has only been demonstrated in simulation, not in reality where complex losses and other non-idealistic conditions exist.

Each section must have a switch, diode, capacitor and an inductor although many of the proposed topologies use pass diodes to allow the use of a single switch. The complexity and losses grow with each additional stage leading to a reduced efficiency [24]. A in-depth theoretical model of a cascaded boost converter is performed in [38]. It is acknowledged that there were practical limitations due to the excessive component count which would cause a geometric increase in circuit complexity for each cascade. It is also stated that as the series of cascades increases the contribution made by each additional cascade to the overall boost voltage decreases [24]. This would mean the circuit complexity and cost added by each additional stage would quickly outweigh the boost benefit given by that stage.

A high-gain quadratic boost converter with voltage multiplier (Figure 1.9) is presented in [39]. It combines the traditional quadratic boost converter and a

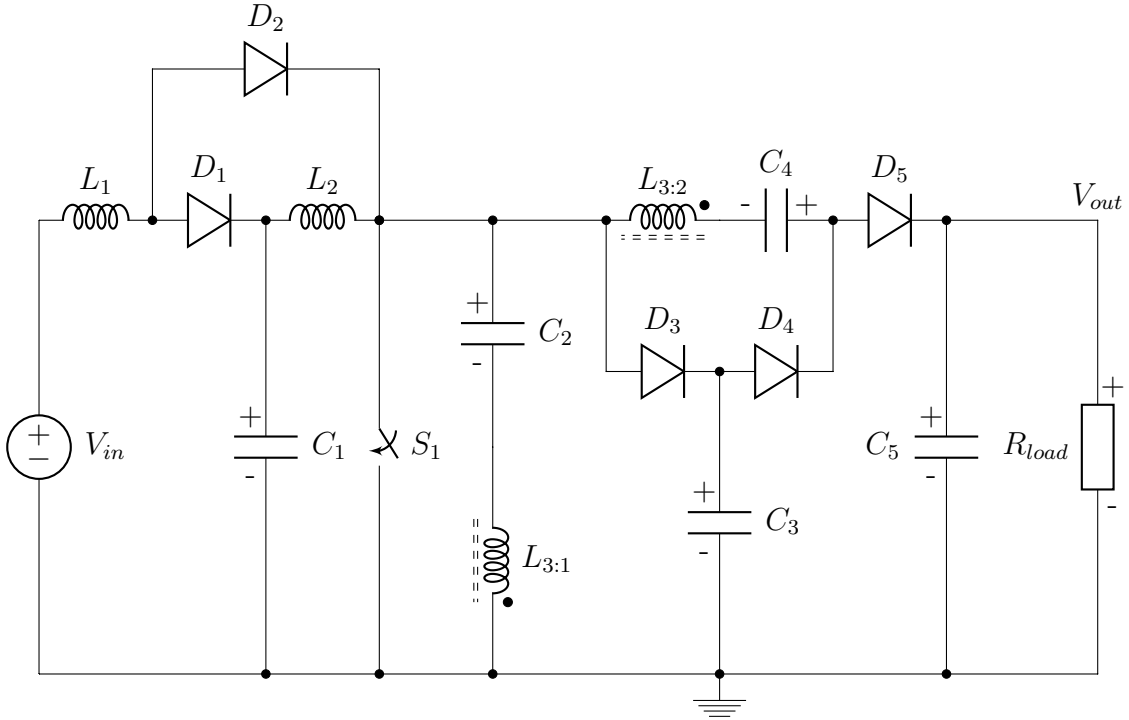


Fig. 1.9: Conventional coupled inductor converter with voltage multiplier circuit [39]

coupled-inductor based voltage multiplier circuit. In Figure 1.9 $C_2, C_3, C_4, D_3, D_4, L_3$ form the voltage multiplier circuit. Much higher voltage gain than the conventional converter can be achieved at the same duty cycle with improved efficiency [39].

It relies on charging and discharging of capacitors to help achieve and maintain the voltage boost. These capacitors will be subjected to high ripple currents as they pass the majority of the power. Low-loss capacitors will need to be used to minimise efficiency reduction from ESR related losses. It is also highly dependant on diodes passing high currents to control the charging and discharging of the capacitors. The measured efficiency was much lower than the calculated efficiency neither of which get above 90%.

1.0.8 Coupled-Inductor-Based Boost Converters

Coupled Inductor-Based converters use a high frequency switched transformer arrangement where the turns ratio is directly responsible for the voltage boost. There are two main variants, Conventional (Figure 1.10) and Flyback (Figure 1.11).

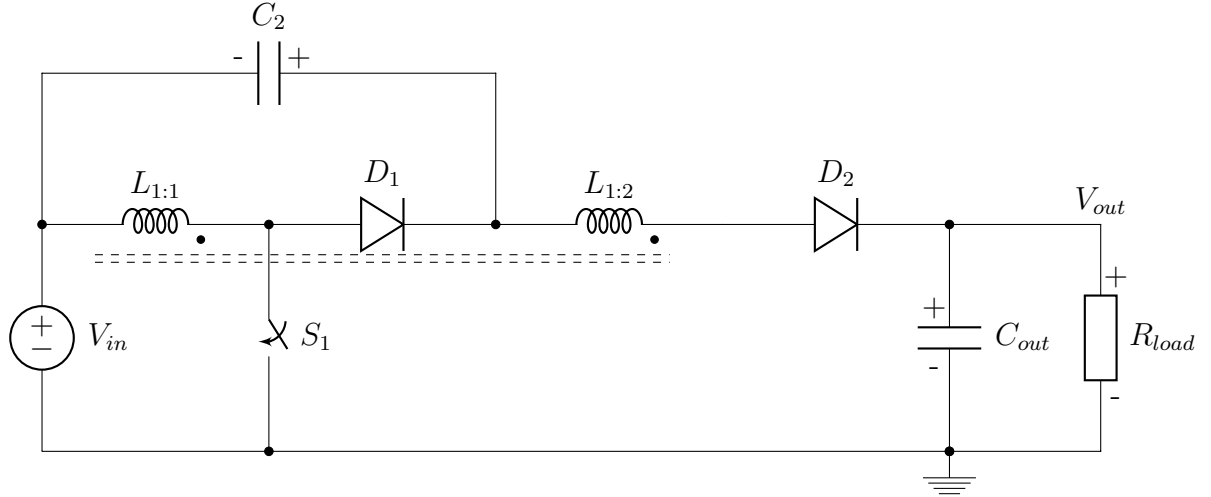


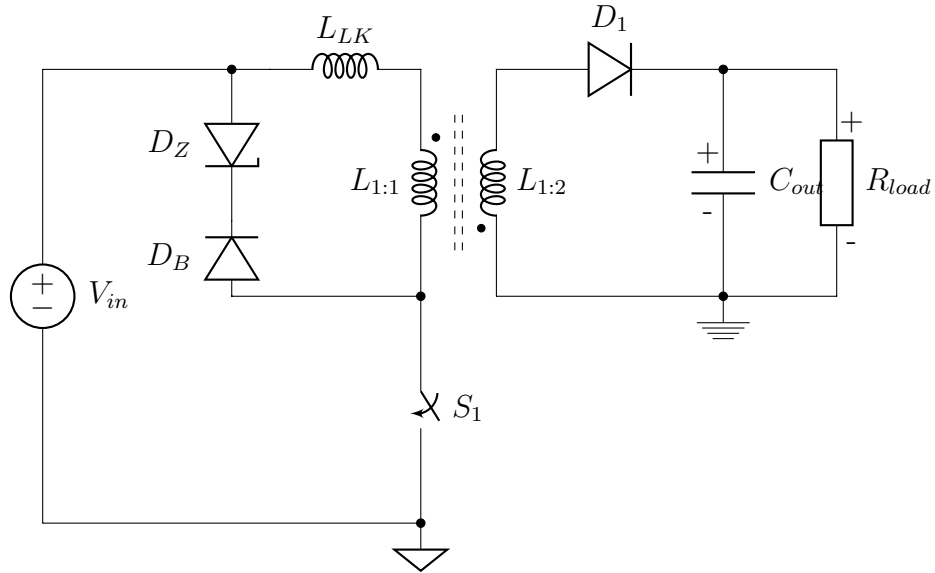
Fig. 1.10: Conventional coupled-inductor boost converter

In the conventional coupled inductor converter (Figure 1.10) the power components are arranged much the same as in the conventional converter with one exception. Instead of the switch being positioned between the inductor and diode, the inductor is split into two windings around a common core and the switch is positioned at the centre-tap. When the switch closes the primary winding $L_{1:1}$ is energised. The secondary winding $L_{1:2}$ cannot pass any current as the output diode D_1 is reverse biased. When the switch opens D_1 becomes forward biased and $L_{1:2}$ now passes current to the output. If the turns ratio of the primary to secondary windings is $1 : N$ then the secondary voltage will be N times the primary voltage.

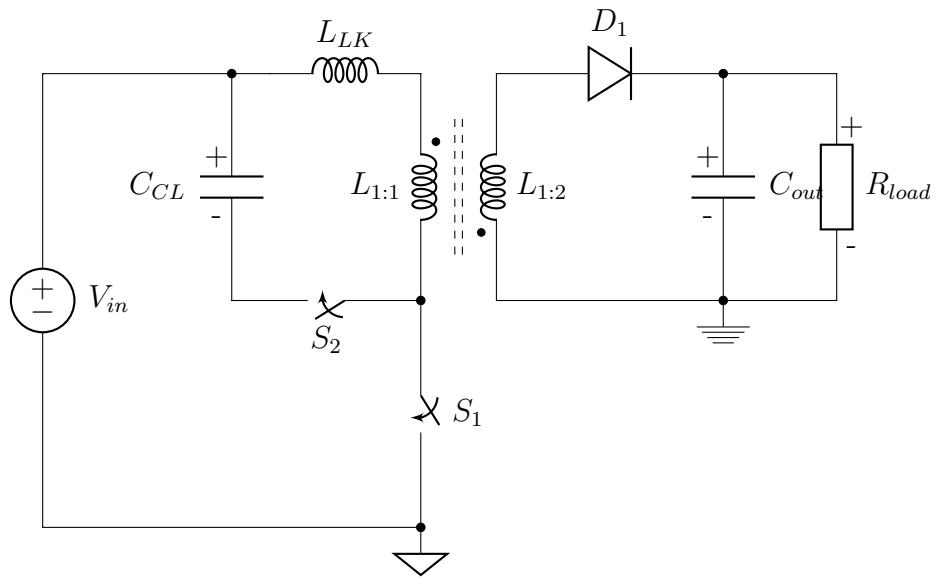
$$V_{out} = N \frac{1}{1 - D} V_{in}$$

This provides the voltage boost without the need for excessive duty cycles.

In Figure 1.11 S_1 closes and charges the primary side transformer coil $L_{1:1}$. Diode D_1 is reverse biased so the energy cannot pass to the load during this state. When S_1 opens D_1 becomes forward biased and allows $L_{1:2}$ to discharge into the load.



(a) Flyback with passive clamp circuit



(b) Flyback with active clamp circuit

Fig. 1.11: A typical Flyback boost converter with clamp circuits

The flyback can also be combined with other topologies to improve the boost ratio while maintaining the benefits of the leakage energy recovery. Figure 1.12 shows a simplified schematic of the flyback combined with the conventional boost converter called a Hybrid Flyback Boost converter [40]. In Figure 1.12 the main

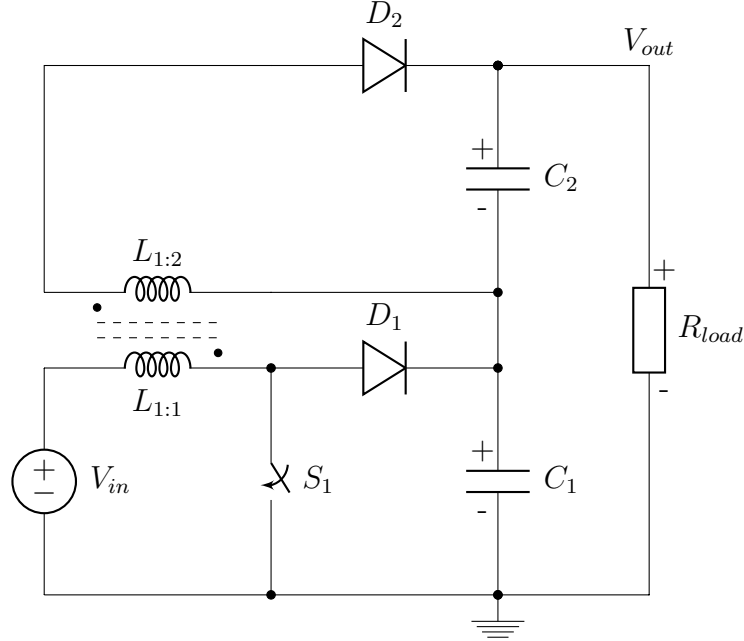


Fig. 1.12: Flyback coupled-inductor boost converter

power components remain in the same arrangement as the conventional boost converter. This charges the output capacitor C_1 following the conventional transfer function

$$V_{C_1} = V_{in} \frac{1}{1 - D}$$

The inductor in this section of the circuit $L_{1:1}$ forms the primary side of the transformer. The secondary winding $L_{1:2}$ produces a separate voltage to charge output capacitor C_2 . If the primary to secondary turns ratio is $1 : N$ then

$$V_{C_2} = N \times V_{in}$$

The secondary winding $L_{1:2}$ is also electrically isolated from the primary meaning all power contributed by that branch of the circuit must transfer through the magnetic core. This introduces magnetic losses depending on the quality of the magnetic core material. High power transfer will require higher quality core material potentially leading to increased costs.

Flyback boost converters have drawbacks at high gain levels [41]. The transformer is not ideal. In accurate modelling a small leakage inductance is present which is

effectively in series with the primary side winding and switch. When the switch opens the stored energy in the primary winding couples through to the secondary winding and supplies the load. The leakage inductance is not coupled so when the current flow is interrupted by the switch opening it generates a large voltage spike which applies voltage stress to the switch.

Voltage stress problems can be ameliorated by the use of a clamping circuit which also improves the efficiency [42, 43]. Active clamp circuits or “Snubbers” are used to dissipate the leakage energy and avoid the generation of the harmful voltage spike. The most simple and inexpensive implementation is the passive clamp circuit (Figure 1.11a) which simply uses two diodes to provide an alternate current path for the leakage energy. When the switch is closed diode D_B blocks so no current flows. When the switch opens and the voltage across L_{LK} begins to rise D_B becomes forward biased and D_Z conducts when the voltage exceeds its zener voltage. This is an inefficient solution as the diodes dissipate the leakage energy as heat. Also the higher the switching frequency the more inefficiency is produced.

Alternately, rather than simply dissipating the leakage energy it can be recycled using an active clamp circuit. In Figure 1.11b S_2 is briefly closed to allow the leakage energy to charge capacitor C_{CL} . The transformer then discharges into the load after which S_2 can then be closed again to allow C_{CL} to discharge through the transformer into the load. Switching S_2 at the right times allows S_1 to switch under Zero-Voltage conditions (ZVC) thus relieving the stresses yet further [42].

The active clamping circuit can also be applied to the conventional coupled-inductor converter [43].

An improved topology was proposed by [42] with minimal increase in complexity. This retains the benefits of coupled inductors and recycles the leakage energy to allow high step-up voltages and greater efficiency than the Active Clamped topology.

Solutions to these problems have been suggested by [41, 44–59] and they can achieve good results but do require a large number of components.

Multiple secondary windings can be used to charge separate capacitors which can then be attached in series to build up a higher voltage as shown in Figure 1.13 from [41]

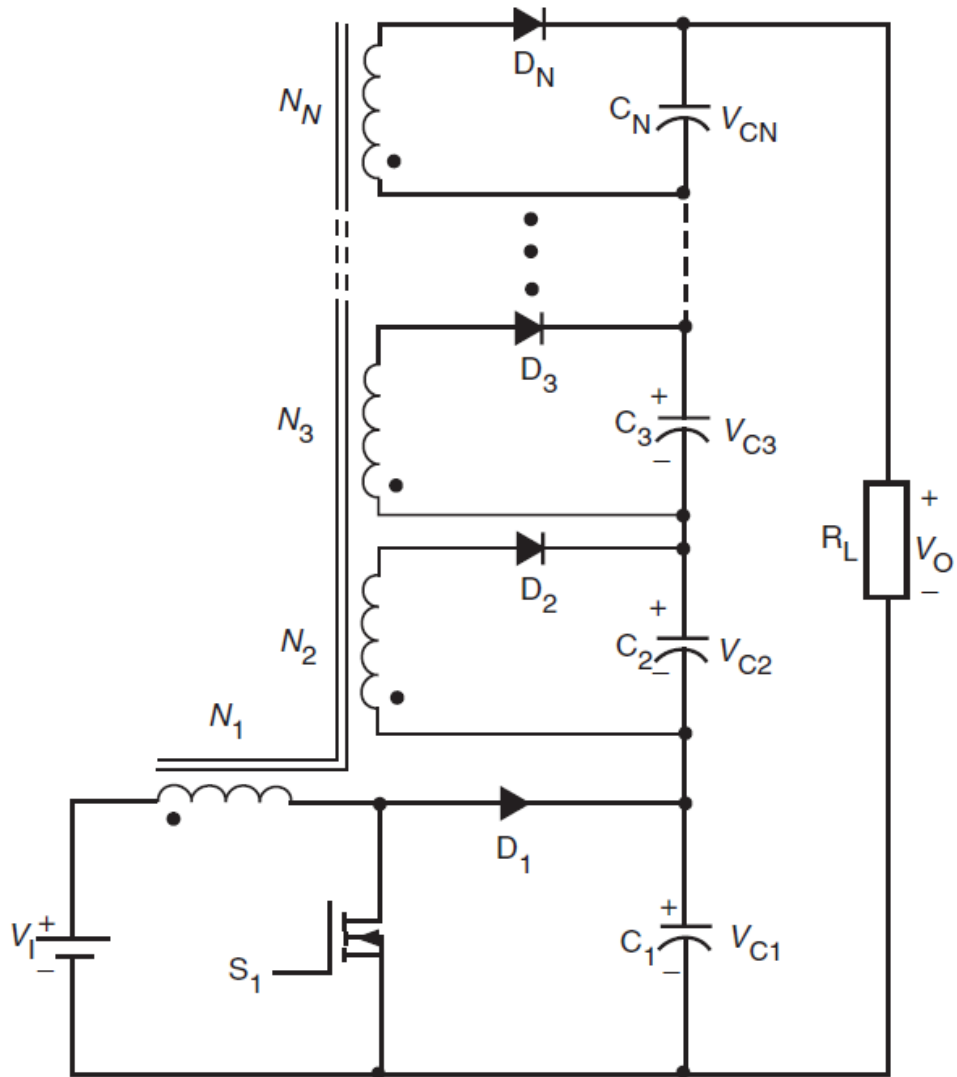


Fig. 1.13: High output voltage Flyback topology [41]

Comparisons of results against the basic boost circuit confirm that the proposed topologies are considerably more effective. The flyback converter can also be merged with the conventional interleaved topology (Figure 1.14) as proposed in [60]. Then a voltage multiplier module (Figure 1.15) can be added for higher

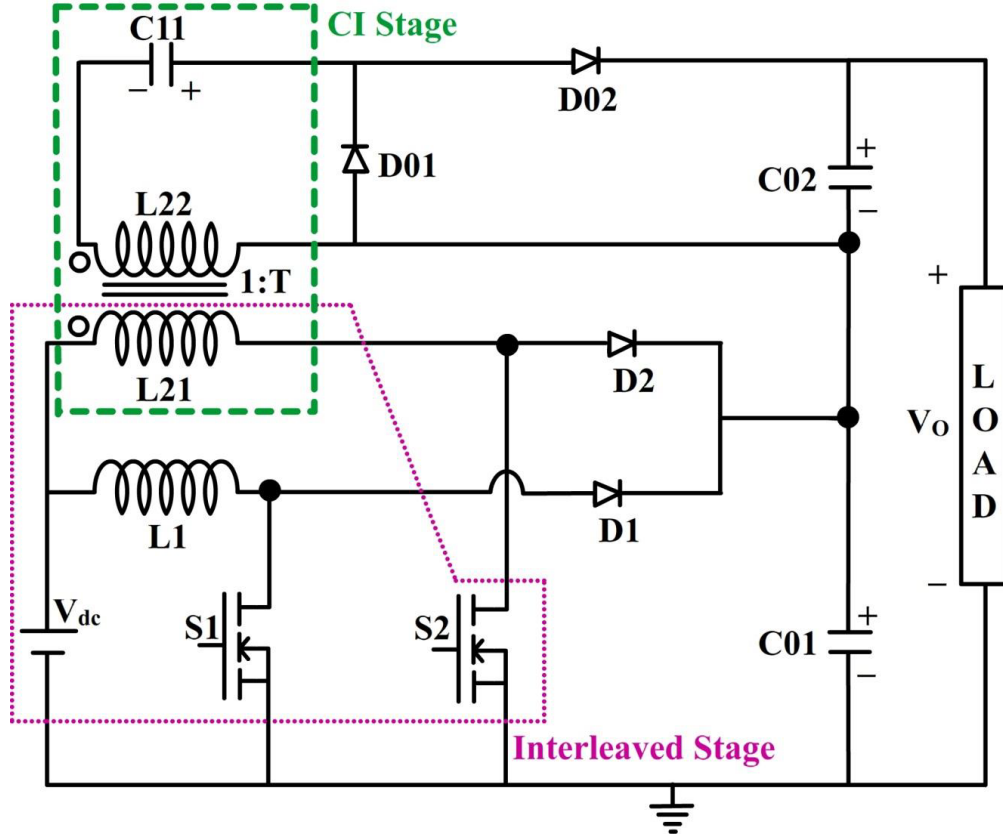


Fig. 1.14: Flyback converter combined with conventional interleaved topology [60]

boost ratio [60]. To generate the voltage multiplication requires replicating the diode-capacitor arrangement several times thus multiplying the associated losses.

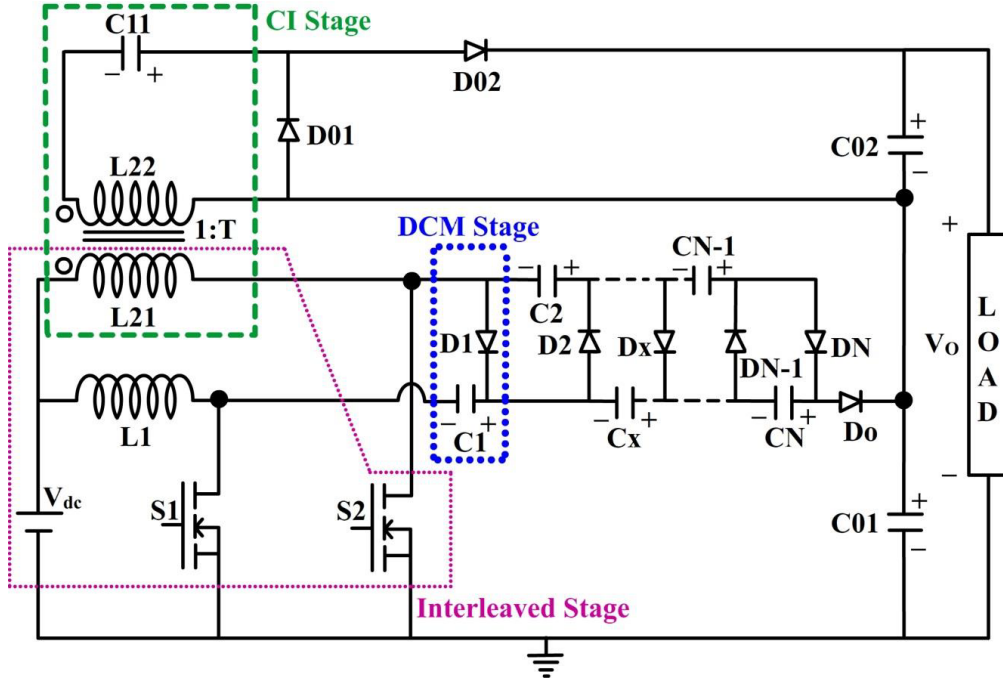


Fig. 1.15: Flyback converter combined with conventional interleaved topology and voltage multiplier cell [60]

A non-isolated Zero-Voltage Switched (ZVS) interleaved boost converter (Figure 1.16) is suggested by [61]. This merges the coupled inductor and conventional interleaved topologies. Rather than simply running two conventional converters in parallel (such as in the conventional interleaved topologies (Figure 1.3)) or coupling the inductor on a single conventional converter stage (such as in the classic coupled inductor topologies (Figure 1.10)) this topology uses coupled inductors to cross-connect the two parallel paths in the conventional interleaved topology.

It incorporates an active clamp circuit to recycle the leakage energy from the coupled inductor and reduce voltage stresses on the switches. It is claimed that $>10\times$ voltage gain is achievable without large duty cycles while maintaining efficiency and validated through experimental results.

If the primary-secondary turns ratio is $1 : N$ then a secondary voltage of $N \times V_{in}$ is produced. The secondary coils are arranged in series to give the voltage boost. There is only one diode and one series capacitor in the main current path. These will need to have low-loss to prevent efficiency reduction. Efficiency above 90% is quoted over a wide power range with a distinct peak of nearly 97% at low power.

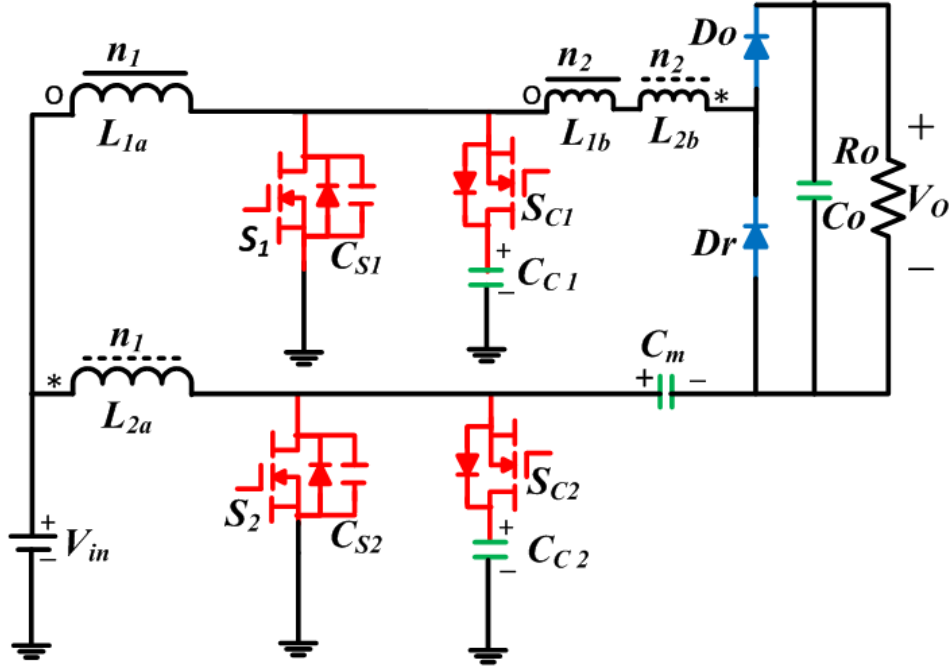


Fig. 1.16: Non-isolated Zero-Voltage Switched (ZVS) interleaved boost converter [61]

This is taken a step further by [62] (Figure 1.17) by adding voltage multiplier stages. In Figure 1.17 there are two transformers L_1, L_2 . The primary windings $L_{1:1}, L_{2:1}$ are switched in an interleaved manner by switches S_1, S_2 respectively. The secondary windings $L_{1:2}, L_{2:2}$ are arranged in series with opposing phases to power the two charge pump circuits individually. When S_1, S_2 are both closed $L_{1:2}$ charges capacitor C_3 through diode D_3 and $L_{2:2}$ charges capacitor C_2 through diode D_2 . When S_1 opens $L_{1:1}$ pushes current through D_1 . C_2, C_3 connect in series so their voltages add to produce the output voltage. Input current ripple and voltage stresses are reduced allowing cheaper components to be used [62]. Energy from leakage inductance is recycled to achieve a higher boost ratio while maintaining efficiency. Efficiency of the proposed circuit was obtained by simulation and also from prototype experimentation. This showed that at around 140W output the efficiency was 95% on the simulation and 93% on the test circuit.

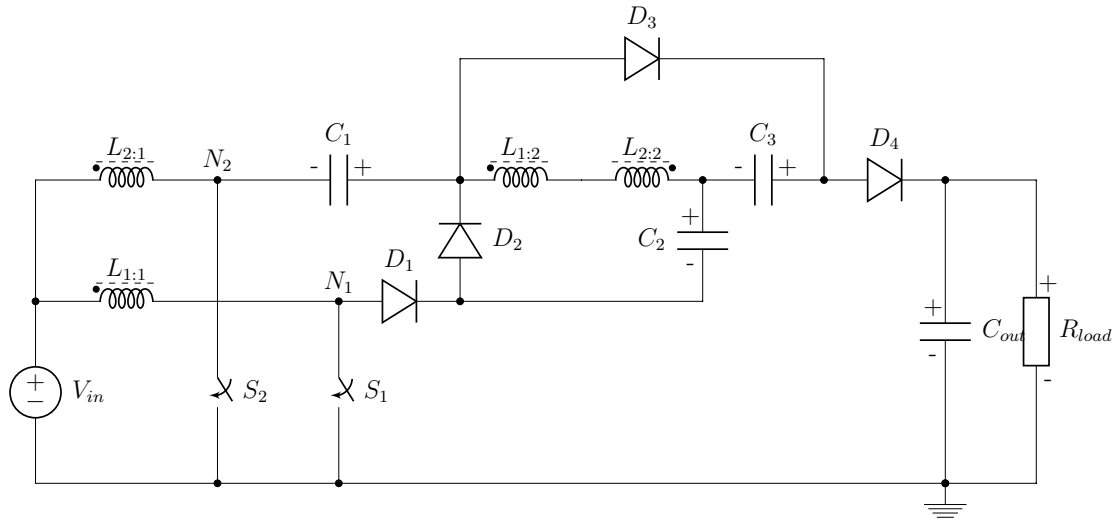


Fig. 1.17: Interleaved converter with voltage multiplier stages [62]

Another version of the coupled inductor interleaved boost converter is offered by [63] in Figure 1.18. This takes the conventional coupled inductor topology (Figure 1.10) and doubles it up to get more boost capability. While it doubles the component count there are no increased voltage or current stresses incurred. The efficiency of the topology was shown to be about 94% at a power output of 140W, this was found by simulation and experiment.

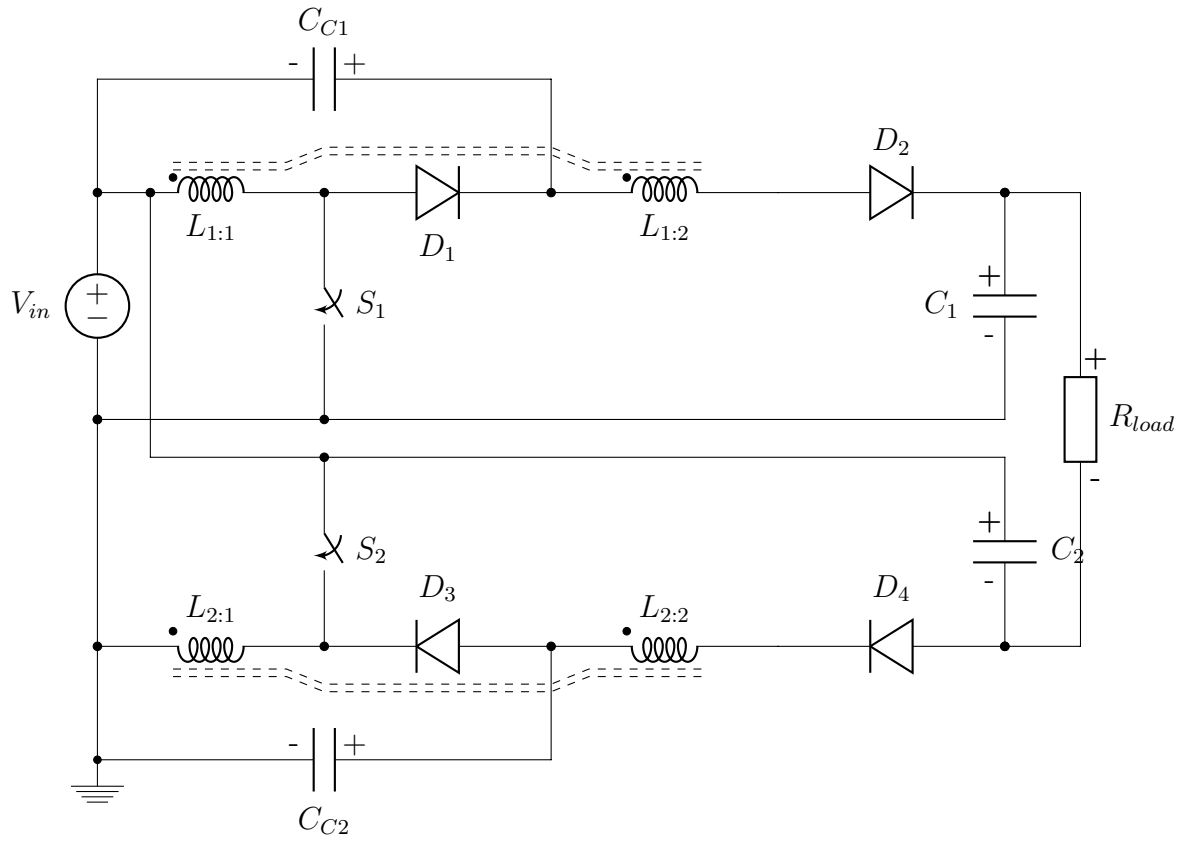


Fig. 1.18: Coupled inductor interleaved boost converter [63]

1.0.9 Switched-Capacitor-Based Boost Converters

A typical switched-capacitor topology is shown in Figure 1.19. Switched-Capacitor converters or Charge Pumps use combinations of switches and capacitors to achieve voltage boosting. The most basic operation is to apply the input voltage across a bank of capacitors connected in parallel which charges them all to the input voltage. Then they are switched into series configuration so their voltages add to form the output voltage [64]. If there are N capacitors in the bank then the basic transfer function would be

$$V_{out} = N \times V_{in}$$

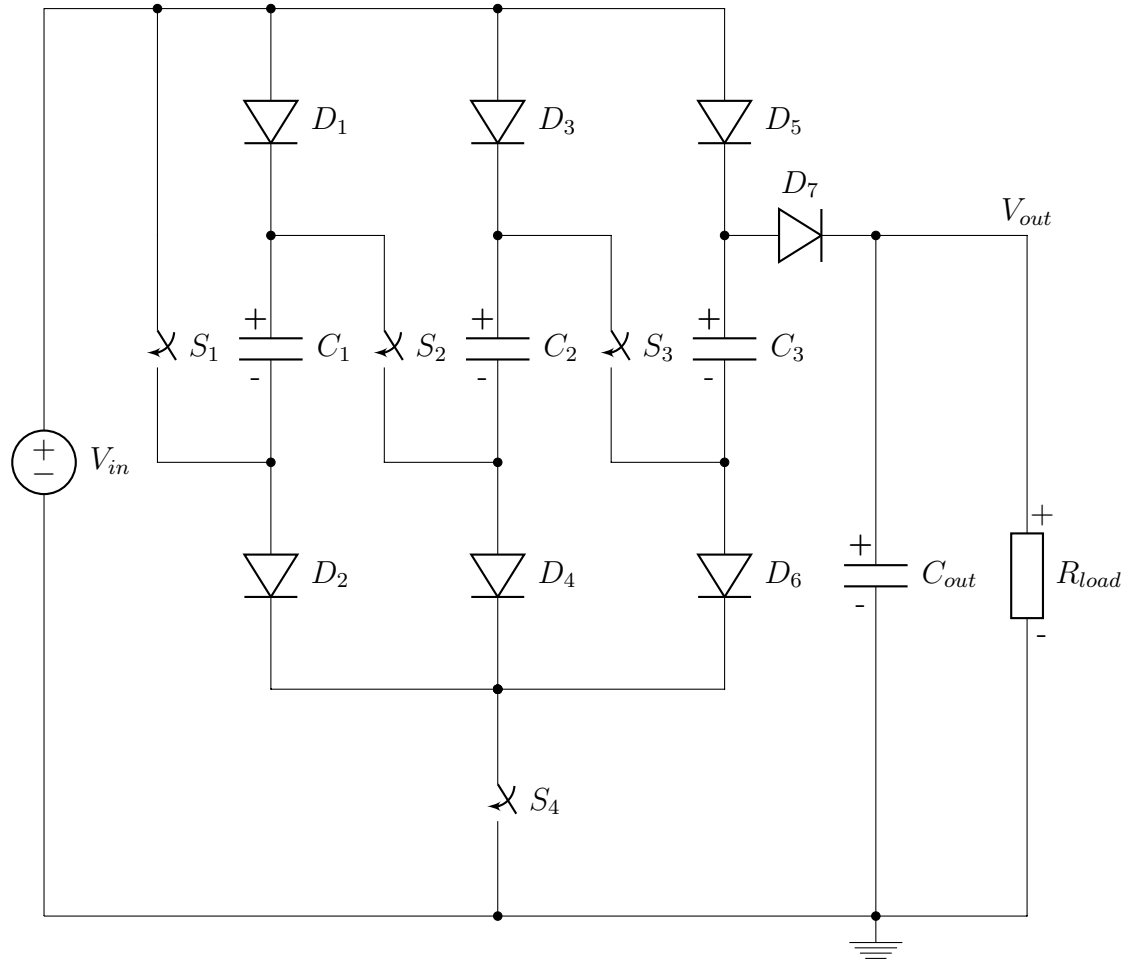


Fig. 1.19: Switched capacitor boost converter

In Figure 1.19 switch S_4 closes and connects all the capacitors to ground in parallel and they charge to a voltage of V_{in} through the forward biased diodes D_1 to D_6 . S_4 is then opened and S_1 , S_2 , S_3 closed so all the capacitors are now connected

end-to-end and their voltages add. In Figure 1.19 there are three capacitors each charged to a voltage of V_{in} and also connected to the supply (also V_{in}) so the voltage at the output will be $V_{out} = 4V_{in}$. They have been widely considered by several researchers [30, 37, 64–66] but the greatly increased component count impacts heavily on their robustness and design elegance [24]. Additionally there will be very large currents involved when continuously charging and discharging large capacitor banks. The current surges at the input when the capacitors are charged could exert large current stresses on the supply as well as the forward conducting diodes and switch.

An early attempt to combine the characteristics of a conventional boost and switched-capacitor converter was proposed in [64]. It follows the basic schematic from Figure 1.19. It was shown to reach a ten times boost by experiment but also showed some difficulty with efficiency when a constant output voltage was required. It was also stated that a higher boost ratio could easily be achieved without impacting on efficiency as “each additional capacitor requires only an additional small transistor and two diodes”. The aim of this implementation was to satisfy an industry requirement of boosting 10x the line voltage with a higher efficiency than a cascade of boost converters which was achieved.

A switched capacitor technique (Figure 1.20) was incorporated into the conventional boost topology by [65]. Here a single switch is used to parallel charge and series discharge a bank of two capacitors to provide a voltage doubling effect at the centre point of the conventional boost circuit.

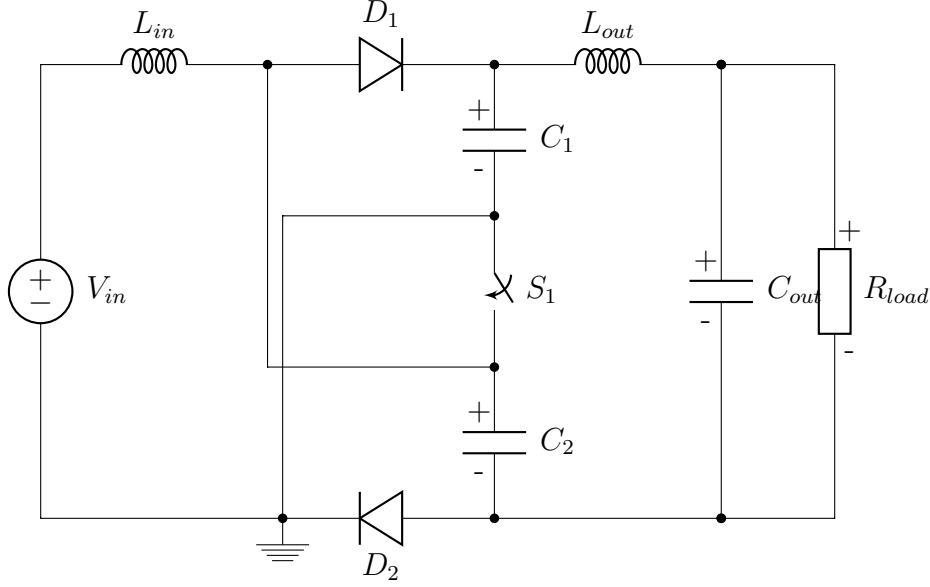


Fig. 1.20: Proposed schematic for conventional boost topology incorporating switched capacitor technique [65]

A new family of boost converters with a basic structure incorporating two capacitors and three diodes is proposed in [66] (Figure 1.21). This could be inserted into circuits in different configurations to allow a higher voltage gain and reduced stresses on the components. This could be applied to several different topologies to improve their performance [66]. The lower voltage stresses allowed the use of better components (MOSFETs and Schottky diodes) that further improved the efficiency of the circuit. The results show a good efficiency of 90% or more at boost values between 5 and 8 times.

A similar concept is proposed in [30] but using two switches and two inductors as their basic network. In Figure 1.22 the inductors are parallel charged series discharged as the two switches both open and close simultaneously.

Using this twin-inductor switching arrangement as a driving base, multiple switched-capacitor (SC) units can be added to boost the voltage (Figure 1.23).

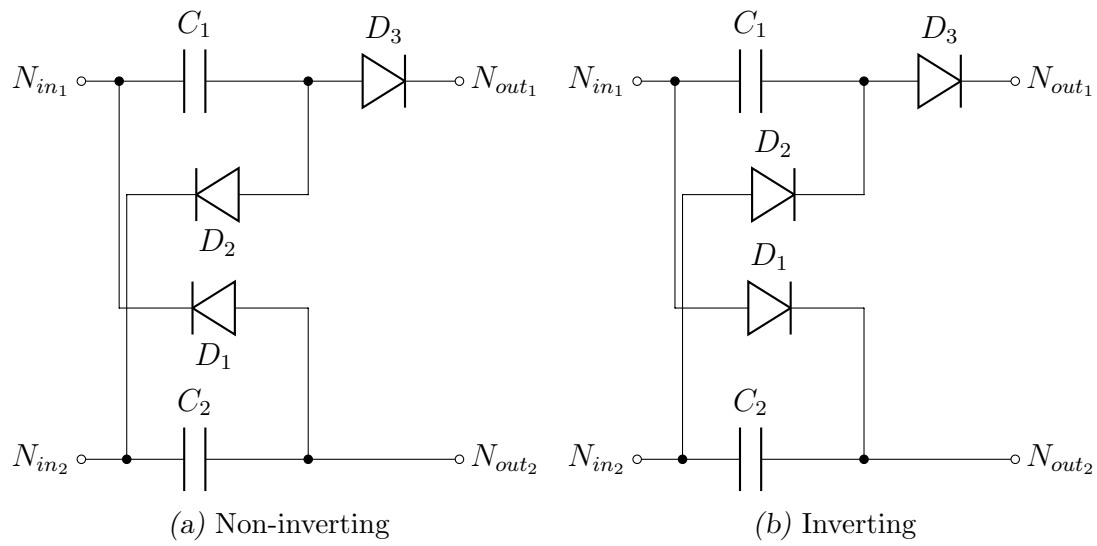


Fig. 1.21: Inverting and non-inverting switched-capacitor (SC) cell [66]

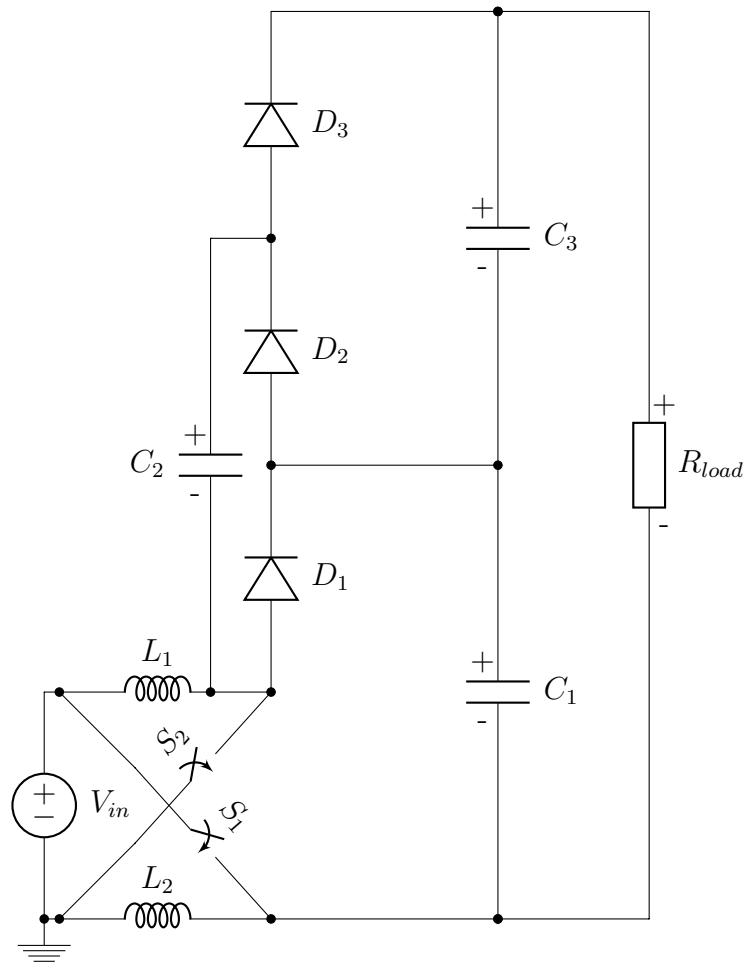


Fig. 1.22: Proposed schematic for switched-capacitor based active network converter [30]

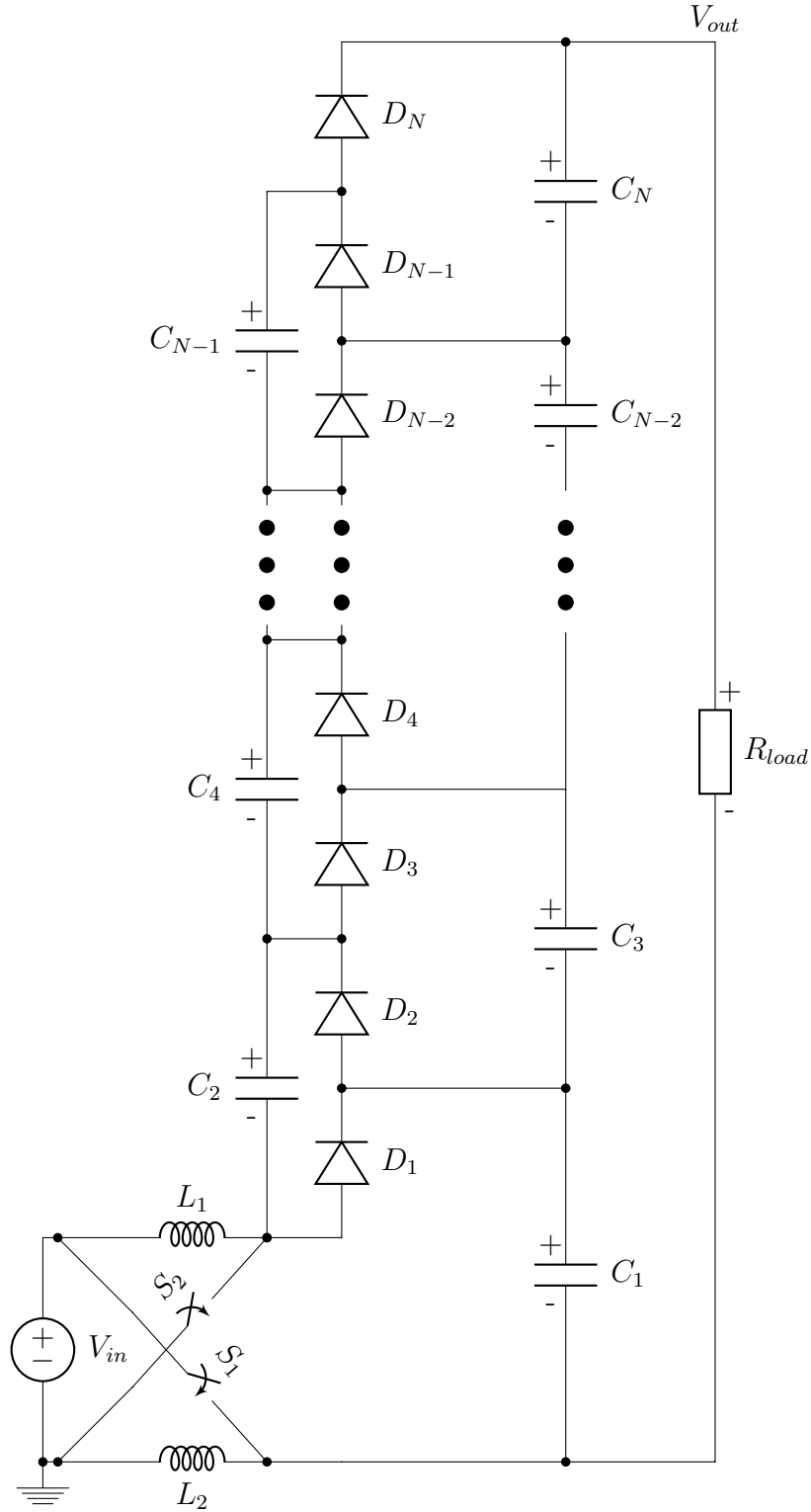


Fig. 1.23: Adapted schematic for switched-capacitor based active network converter [30]

A novel high step-up DC-DC converter using switched capacitor techniques is proposed in [47]. In Figure 1.24 the conventional coupled inductor topology is modified to incorporate a switched capacitor clamp to act as a regenerative snubber. It is technically a passive clamp but uses switched capacitors to recycle the energy. Unlike an active clamp the switching of the capacitors is controlled using passive components (diodes) instead of active switches. This makes it a active/passive hybrid. As a result the voltage stresses exerted on the switch is only $\frac{V_{out}}{7}$ at a boost ratio of around 8x and a measured efficiency of around 96% is achieved. Switched capacitor techniques cause loss in the switch due to high

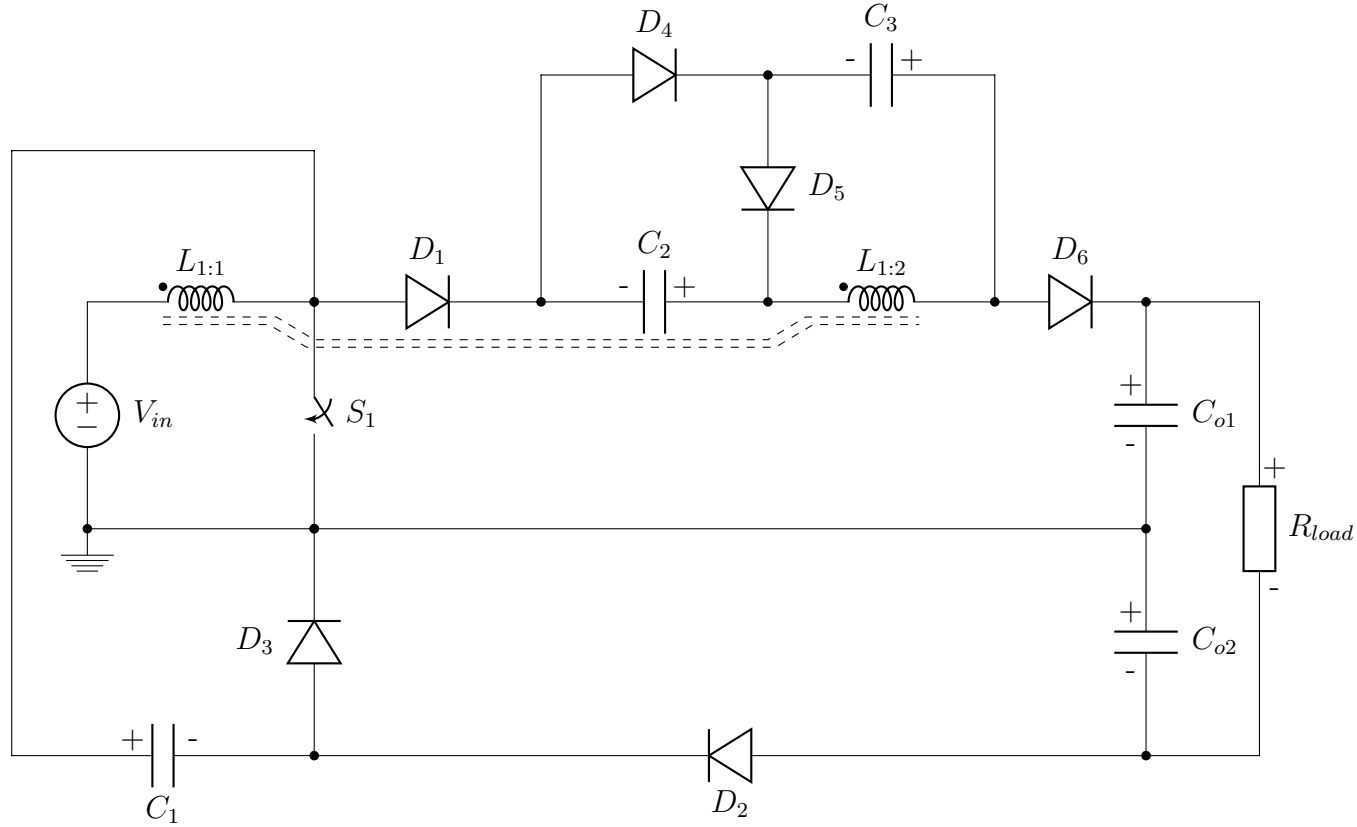


Fig. 1.24: High step-up DC-DC converter using switched capacitor techniques [47]

transient currents and voltage lift techniques (similar to CuK and SEPIC) cause large stresses on the capacitors [47]. Even though a maximum efficiency of 96% is recorded, power has to travel through several ‘Storage & Release’ stages as it travels from the input to the output all of which introduce losses which require expensive low-loss components to counteract.

1.0.10 Interleaved Boost Converters

High Voltage Gain Interleaved Boost Converters are again sub-divided into Voltage Doubler Interleaved Boost Converters and Interleaved Boost Converters Using Voltage Multiplier Cells. A simple voltage doubler interleaved boost topology is shown in Figure 1.25. Voltage doubler interleaved boost converters combine the conventional interleaved topology (Figure 1.3) with a single voltage multiplier stage.

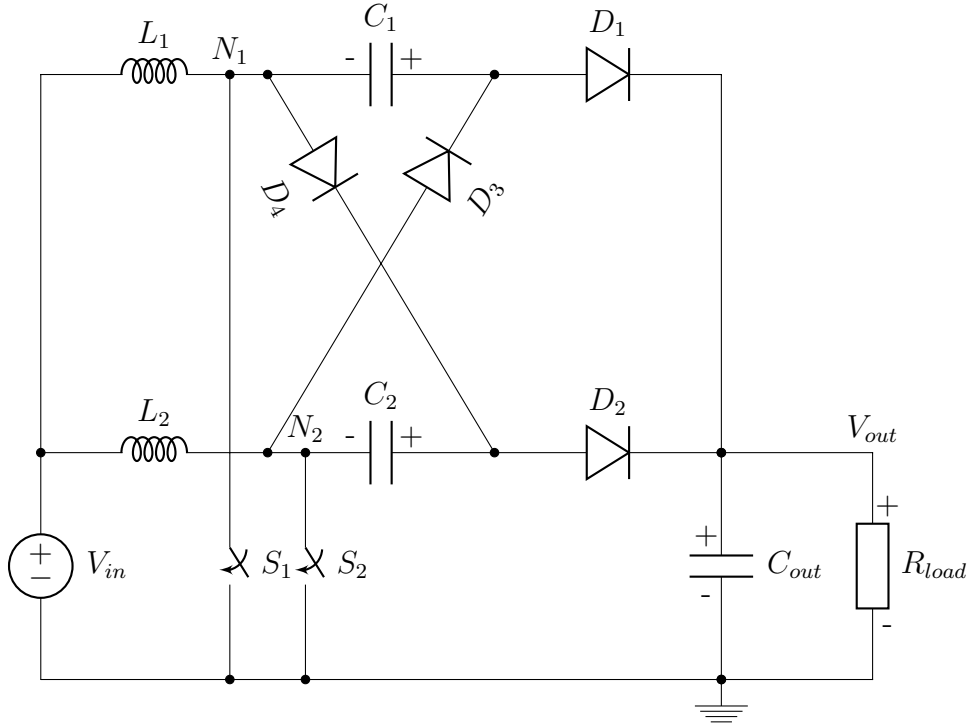


Fig. 1.25: Voltage Doubler Interleaved boost converter

A voltage doubler circuit is a form of rectifier which produces a DC output equal to 2x the AC input amplitude. In Figure 1.25 switches S_1, S_2 are both closed initially. Only one switch opens at a time. When S_1 opens the voltage at node N_1 becomes $V_{N_1} = V_{in} \frac{1}{1-D}$ while $V_{N_2} = 0$ because S_2 is closed. When S_2 opens the voltage at node N_2 becomes $V_{N_2} = V_{in} \frac{1}{1-D}$ while $V_{N_1} = 0$ because S_1 is closed. These two nodes then form the input of the voltage doubler section. If the effective AC input to the voltage doubler circuit is given by

$$V_{AC} = V_{N_1} - V_{N_2} = \pm V_{in} \frac{1}{1-D}$$

this will produce a DC output which is double the AC amplitude

$$V_{out} = 2V_{in} \frac{1}{1-D}$$

Voltage multiplier cells (Figure 1.26) operate in much the same way but use multiple voltage doubling stages such as a Cockcroft-Walton multiplier ladder [67–69]. If there are P multiplier stages then the theoretical transfer function would be

$$V_{out} = 2^P (V_{N_1} - V_{N_2}) = 2^P V_{in} \frac{1}{1-D}$$

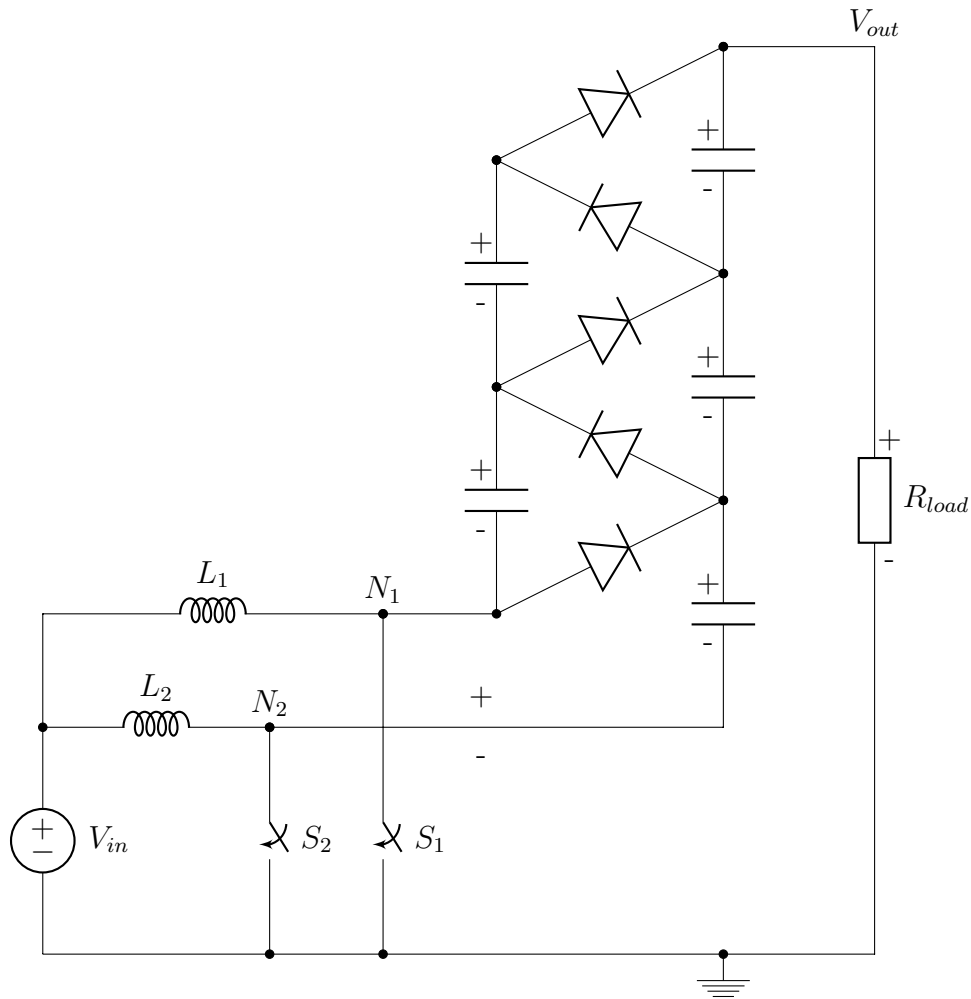


Fig. 1.26: Interleaved boost converter with voltage multiplier cells

Work involving this topology has been presented in [31, 61–63, 70–77].

A voltage doubling topology was put forward by [70] (Figure 1.27) but was improved upon by more effective systems [71, 72] to include automatic current sharing capability without addition of complex circuitry (Figure 1.28). The transformer in [70] has a one to one turns ratio that couples the boost inductors so they conduct an equal current. This has the effect of ensuring that there is no stored energy in the inductors at zero duty cycle thus reducing the effect of output current ripple and easing the load regulation. This is achieved in [71, 72] without the transformer.

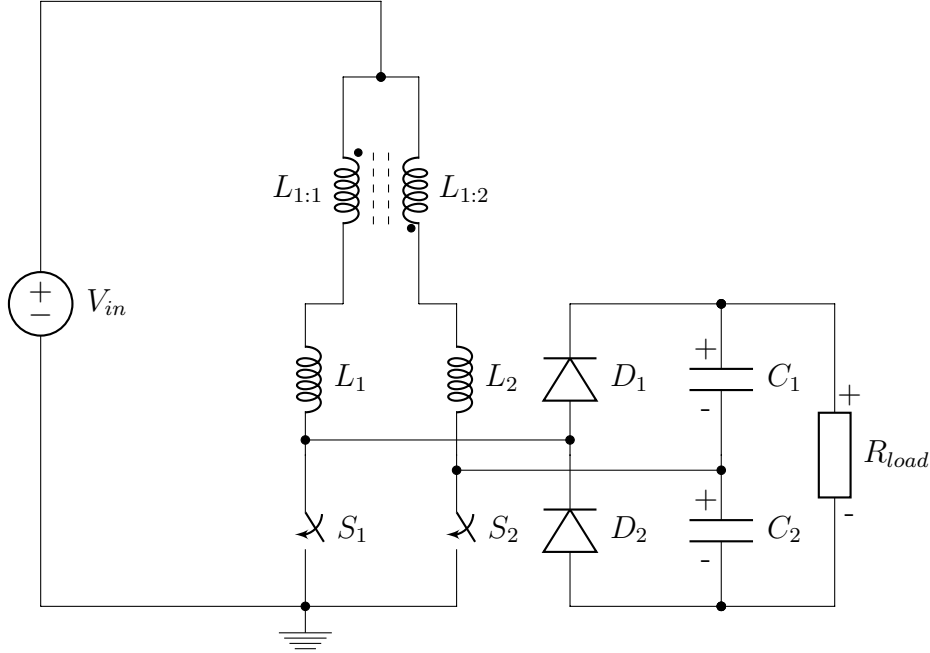


Fig. 1.27: Voltage doubling interleaved topology [70]

The voltage stress across the active switches and diodes is reduced greatly resulting in enhanced efficiency at a voltage gain four times that of conventional converters [72]. Comparisons to the DC-DC flyback converter are made which provides high step-up voltage gains without extremely high duty cycles.

A simulated model and analysis is provided in [72] and showed an efficiency increase from 87% to 94% by replacing diodes with MOSFETS. This complements results from [71] where the peak efficiency rose from 96% to over 97% by replacing certain diodes with active switching components. This proves that conducting diodes in high current paths create losses. MOSFETS have lower loss but also require driving circuitry adding complexity and cost. Simulation results showed that a 16x times boost was possible with an efficiency of 87.4% [72] but this can be improved by replacing the diodes with MOSFET switches. It would be necessary to run an experiment using the MOSFET switches to see if the claimed efficiency increase to 94.2% is obtained with the same voltage boost.

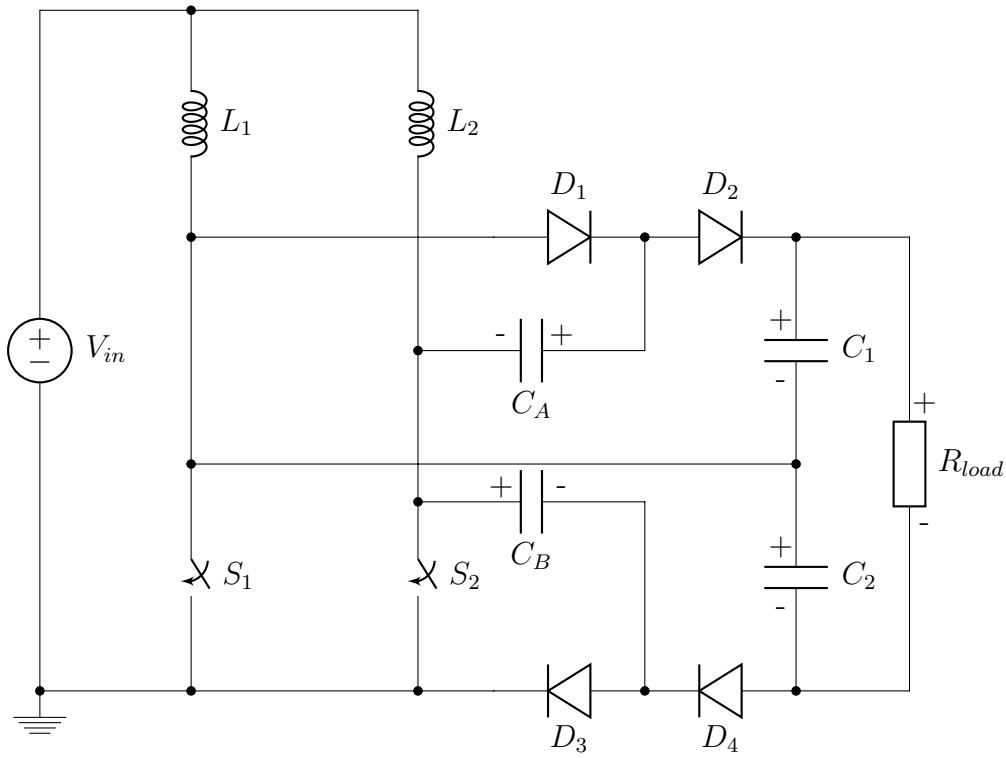


Fig. 1.28: Improved voltage doubling interleaved topology [71,72]

In 2007 [70] amended their own work and proposed a modified interleaved boost converter (Figure 1.29) with voltage doubling as part of a rectifier circuit [78]. It can be implemented in AC-DC conversion applications with the ability to perform power factor correction.

Unlike the earlier proposal this merely doubles the boost ratio rather than a four times boost. Efficiency peaks around 96% but does show the expected steady fall with increasing power output. In Figure 1.29 the capacitor labelled C_B is used as a reservoir to assist with the voltage gain. It is subjected to large transient currents and so low-loss will be important.

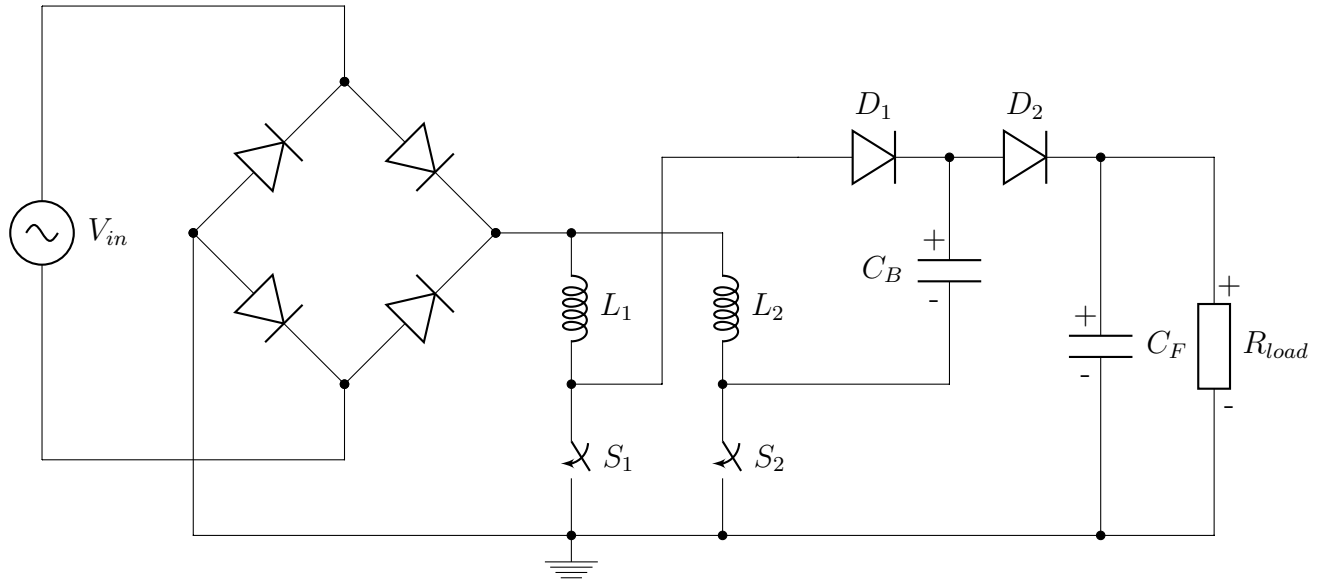


Fig. 1.29: Modified interleaved AC-DC converter with Power Factor correction ability [78]

Using Voltage Multiplier Cells (VMCs) offers the possibility of smaller size components and minimal voltage stress. The interleaved approach also allows for use in high current applications where topologies have been proposed and developed [73, 74]. A multi stage capacitor multiplier (Figure 1.30) is proposed in [73, 74] .

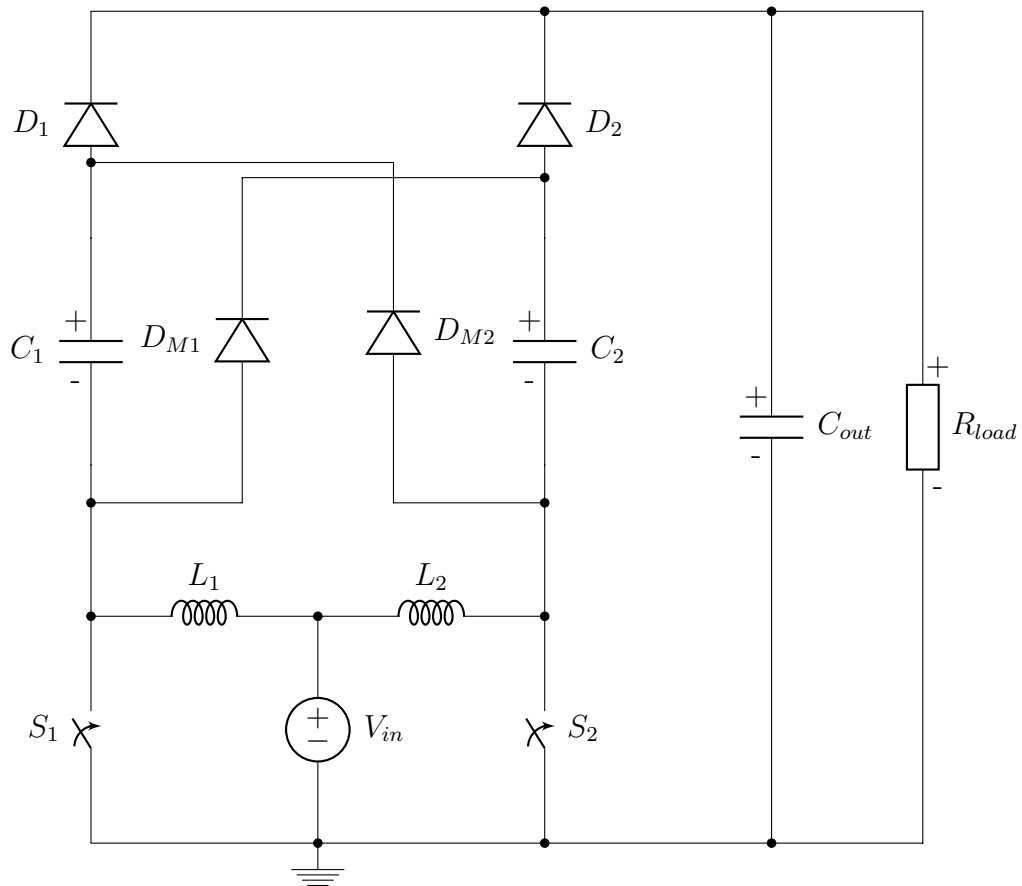


Fig. 1.30: Multi-stage capacitor multiplier [73, 74]

A family of interleaved DC-DC converters for both step-up and step-down applications is proposed by [19] (Figure 1.31). Again it is based mainly on the conventional interleaved topology (Figure 1.3) and incorporates cross-coupling of the windings between the two transformers, known as Winding-Cross-Coupled-Inductors (WCCIs), to alleviate switch voltage stresses by recycling leakage energy.

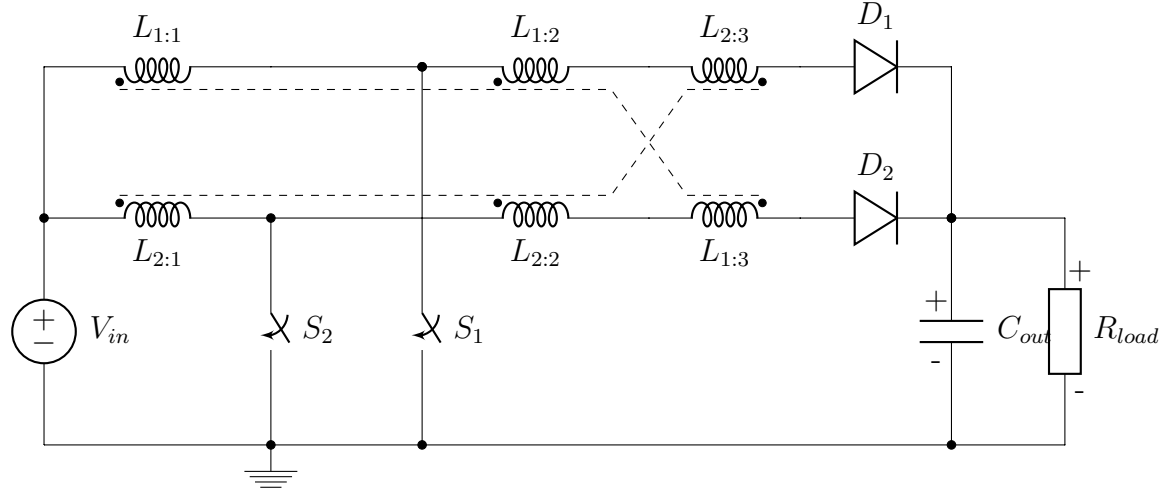


Fig. 1.31: Proposed WCCI topology [19]

1.0.11 Three-State Switching Cell (3SSC) Based Converters

The topology proposed by [70] in Figure 1.27 uses a transformer to balance the input current. The same principle led to the introduction of the autotransformer which is the heart of the 3SSC converter. The 3SSC consists of a standardised arrangement of an inductor, an autotransformer and four switches as shown in Figure 1.32. This can be implemented as a driver for various voltage multiplying topologies.

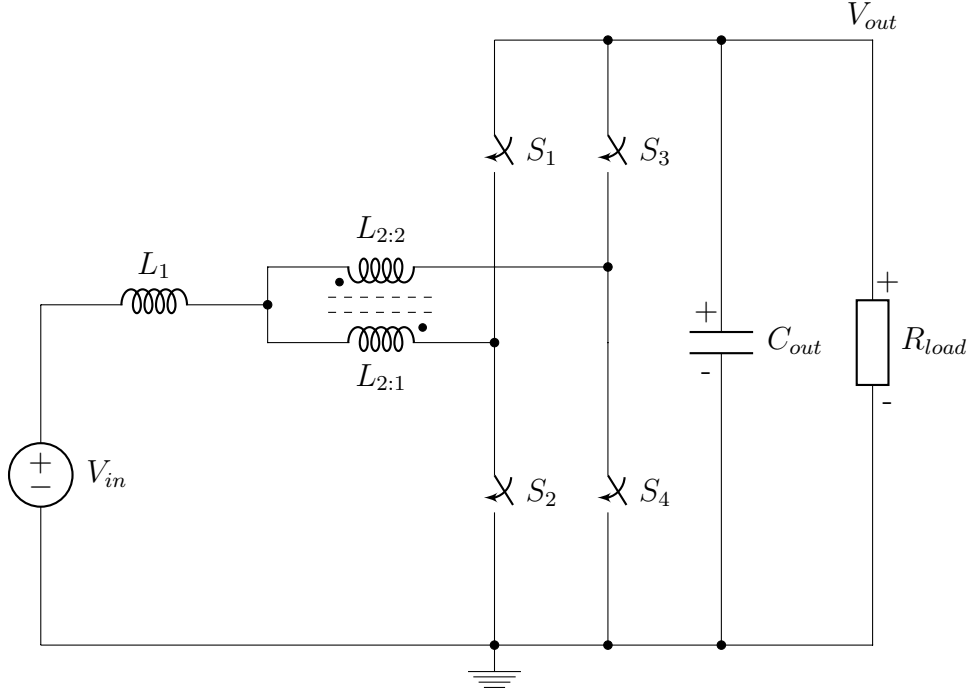


Fig. 1.32: Three-State-Switching-Cell (3SSC) boost converter

In Figure 1.32 $L_{2:1}$, $L_{2:2}$ make up a current balancing autotransformer. S_1 and S_3 can be replaced by diodes to form two switch-diode pairs. Without the autotransformer this is basically the conventional boost converter with a switch in place of the forward conducting diode. The purpose of the transformer is to allow a current path for the active coil to eliminate the voltage spikes which occur when the switches open. In Figure 1.32 switches S_2 , S_4 close together. Only one of them opens at any time and their respective partner switches S_1 , S_3 are switched in complement with them. Initially S_2 , S_4 are closed and L_1 charges through the transformer. When S_2 opens S_1 closes and L_1 discharges through $L_{2:1}$ and S_1 into C_{out} . Normally S_2 would be subjected to a voltage spike when it opens as there is a finite delay time between S_2 opening and S_1 closing where the current path for L_1 is disconnected. However, because S_4 is still closed providing an alternate current

path through $L_{2:2}$ during this tiny delay period, the generation of the voltage spike is avoided.

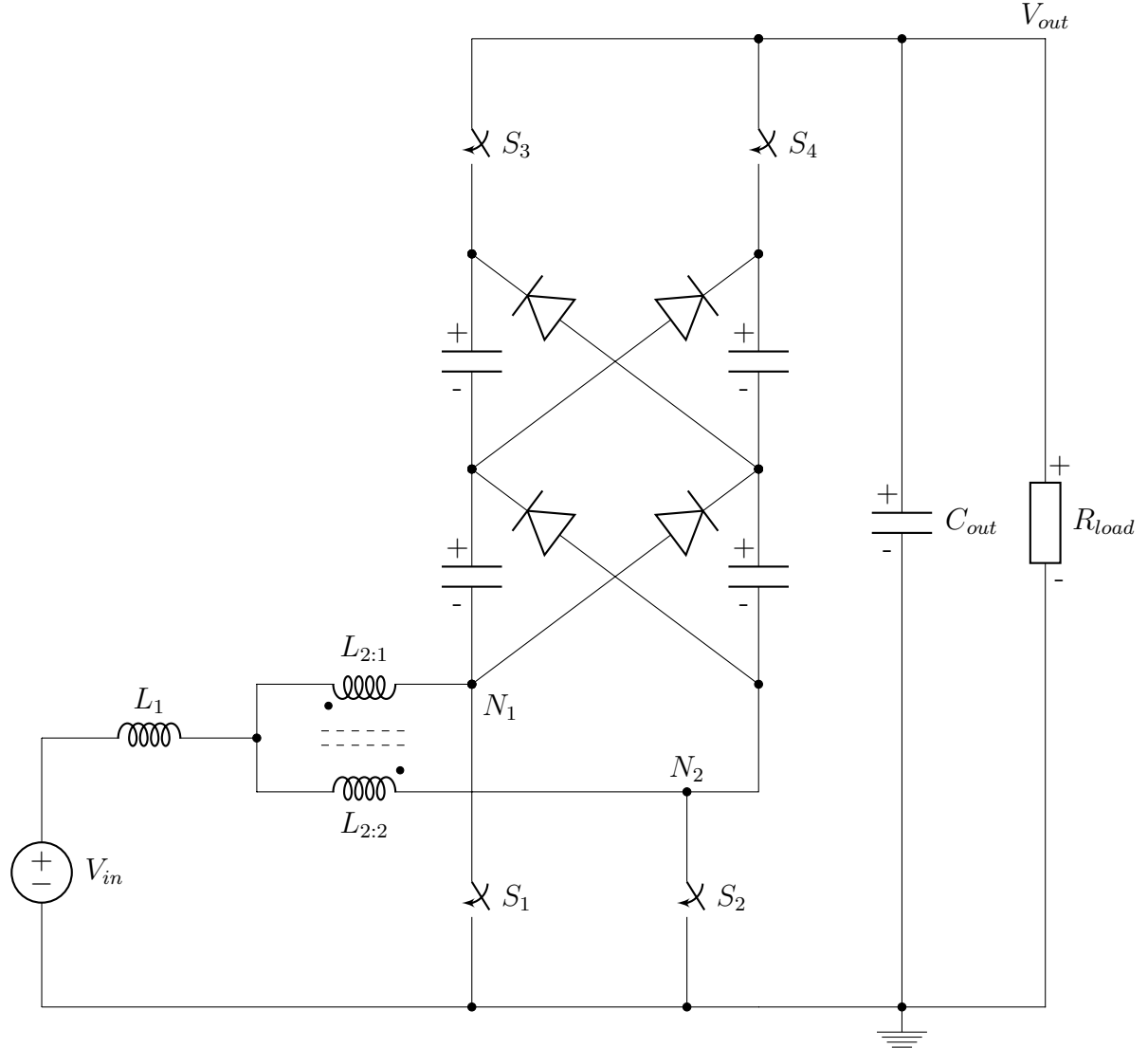


Fig. 1.33: Three-State-Switching-Cell (3SSC) boost converter with Switched Capacitor (SC) voltage multiplier cells

Recent topologies such as Interleaved and 3SSC all appear to be converging on the same principle of using an autotransformer [70, 73, 74, 79–82]. The 3SSC converter uses an autotransformer to allow the circuit current to self-balance and clamp switch voltages to relieve stresses. It also uses secondary windings on the autotransformer in place of the VMCs to produce high voltage gain while keeping voltage stresses on switching components low. This is essentially a cross between

the conventional coupled inductor converter and the interleaved converter; very similar to the Weinberg topology which is covered in more detail in Section 1.0.12.

Work involving this topology has been presented in [25, 82–97]. All use the classic 3SSC current-balancing autotransformer arrangement in combination with a variety of boosting methods to generate the voltage boost. Two of the most common are the voltage multiplier cell [84, 96] and much more popular coupled inductor [25, 83, 85–90, 94, 97].

Only a small variety of 3SSC based boost converters have been developed. One of which is using a multiphase transformer (Figures 1.34, 1.35, 1.36). By coupling the energy through multiple windings on the same core the power can be split into several parallel paths to alleviate switch stresses [25].

In Figure 1.34 there are three switch pairs S_1S_2 , S_3S_4 , S_5S_6 . The two switches that make up each pair are switched in compliment. They must never switch together otherwise the load will be shorted to ground. The three pairs switch in sequence. In each case the active coil passes power to the output while the other two provide a path for the leakage energy and also prevent the storage inductor L_1 from saturating and causing the converter to enter discontinuous mode.

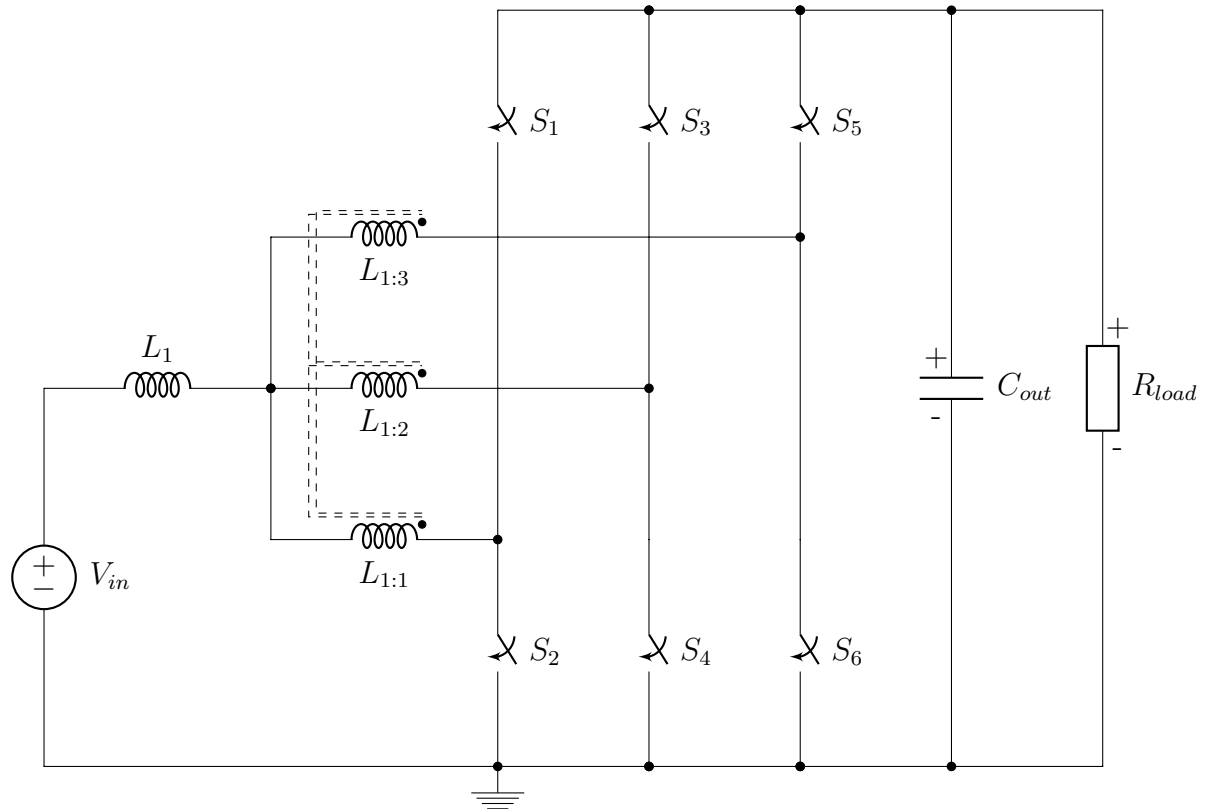


Fig. 1.34: 3SSC based multiphase switching cell [25]

In Figure 1.35 if switches $S_7 \cdots S_{12}$ are switched the same as $S_1 \cdots S_6$ the coupled secondary windings generate a second copy of the output voltage which is electrically isolated. It is then attached in series with the original output so the voltages add together and the load is positioned across both. Furthermore if the ratio of $L_{1 \cdots 3}$ to $L_{4 \cdots 6}$ is $1 : N$ then the secondary voltage can be made larger than the original by a factor of $1 : N$.

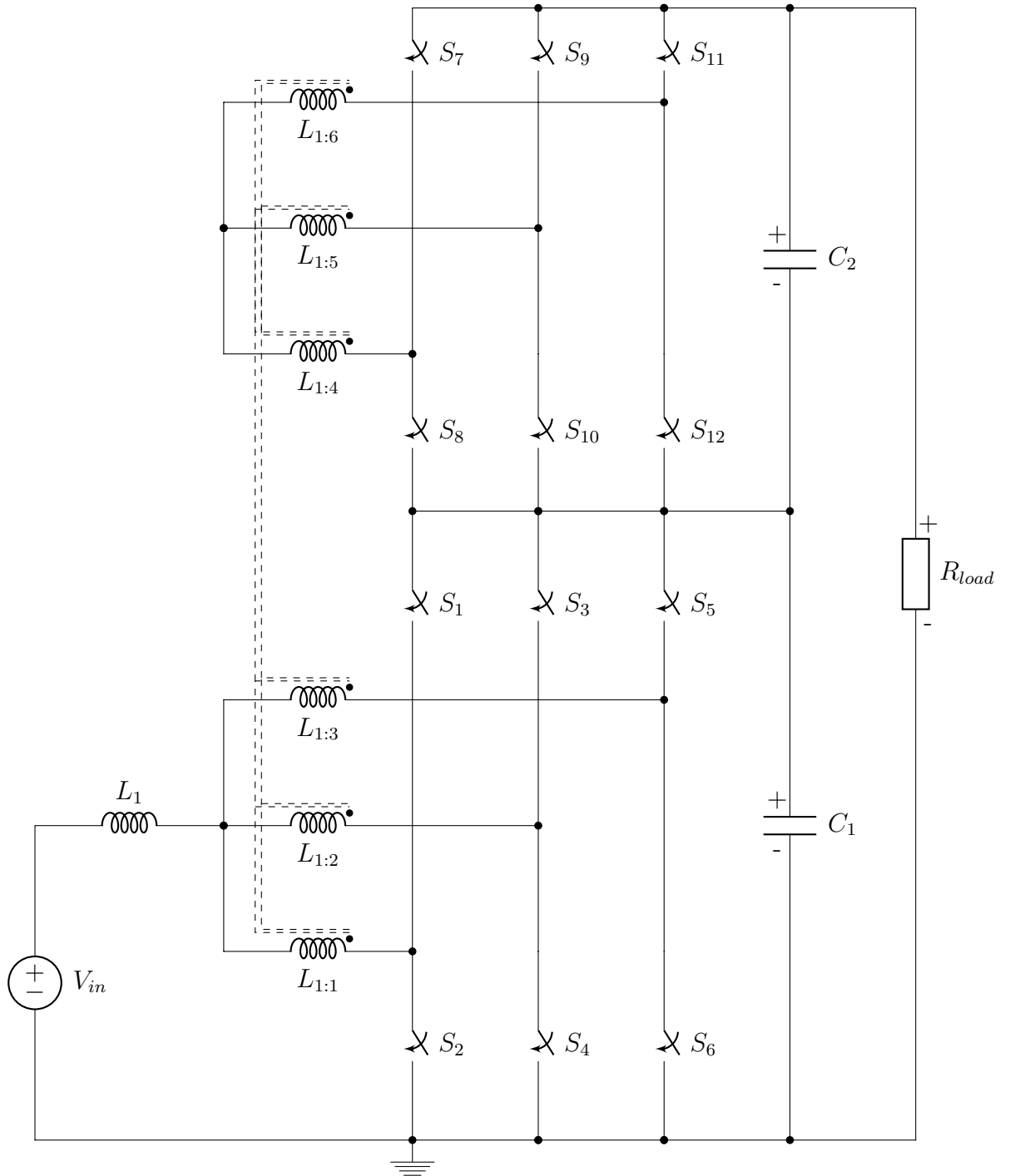


Fig. 1.35: 3SSC based coupled multiphase switching cell [25]

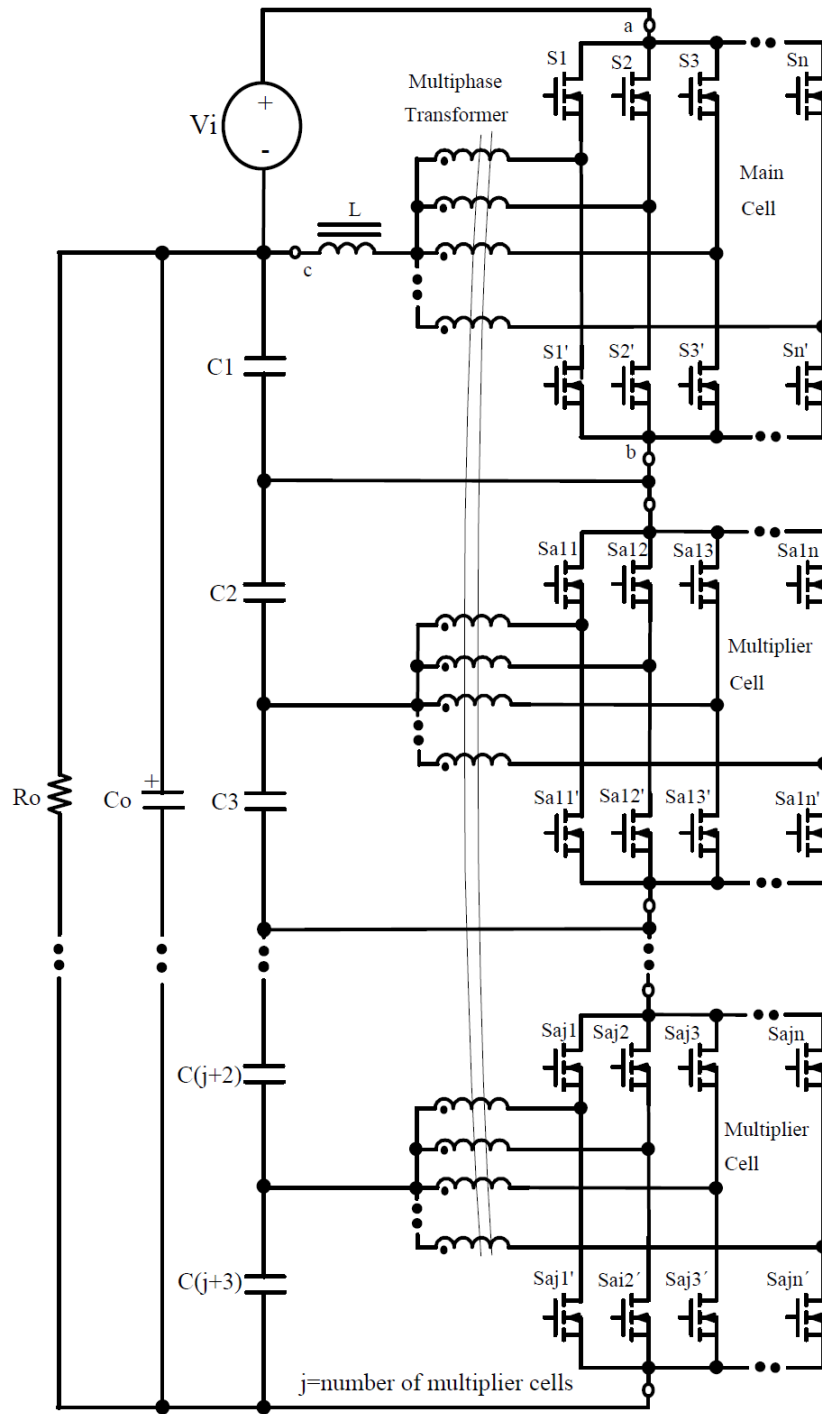


Fig. 1.36: 3SSC multiphase coupled [88]

Instead of switching the transformer coils actively, some topologies simply rectify the output on the secondary side of the autotransformer to charge capacitors which are then connected in series to generate a higher voltage (Figure 1.37).

Additionally the coupled transformer can be used to manage power throughput in DC bus connections. In Figure 1.38 the autotransformer forms a bridge between a load and multiple sources. The switching can be controlled to manage power delivery to the load or between the two sources.

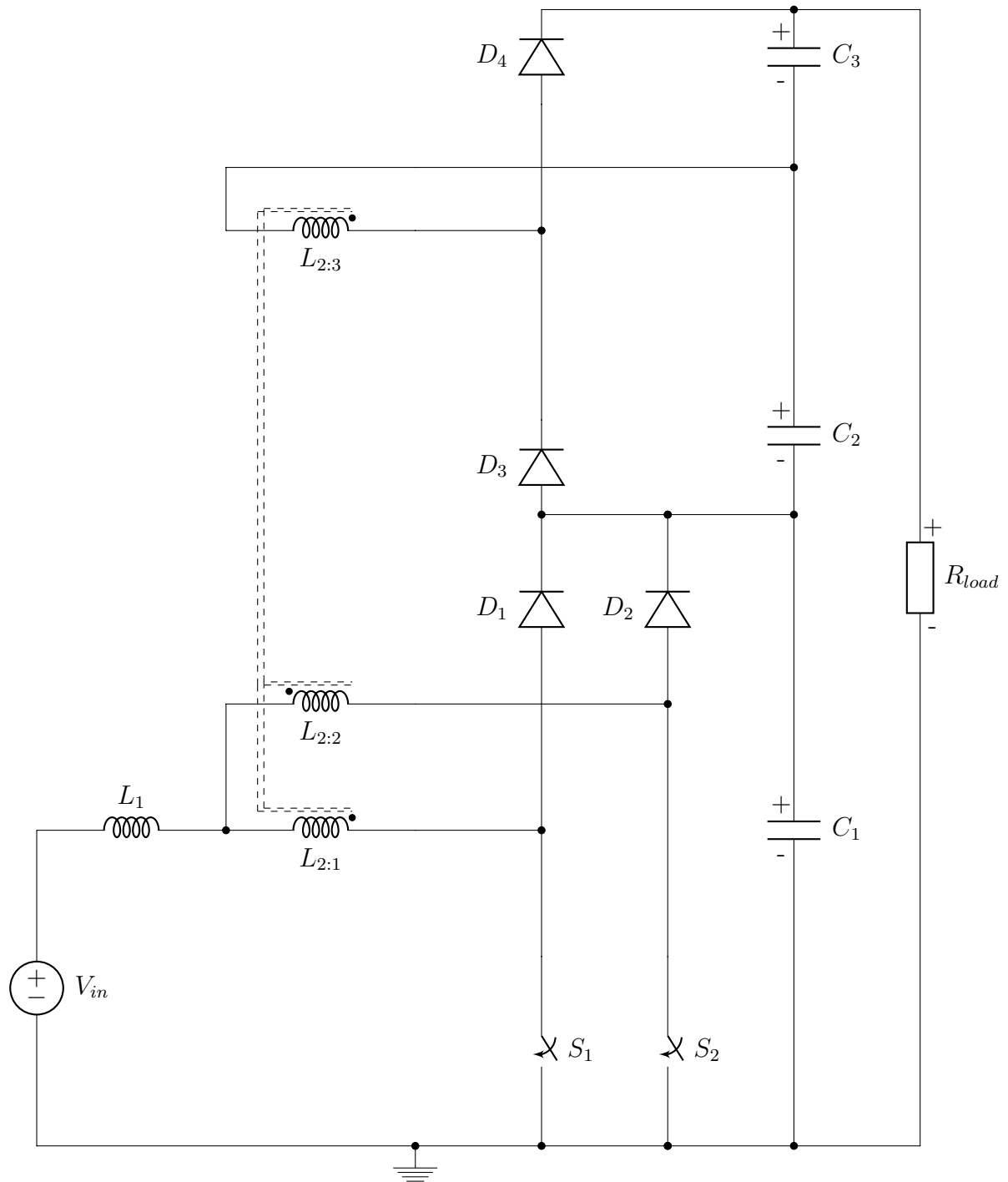


Fig. 1.37: 3SSC based multiphase voltage multiplier using switched capacitors [83, 89, 90, 97]

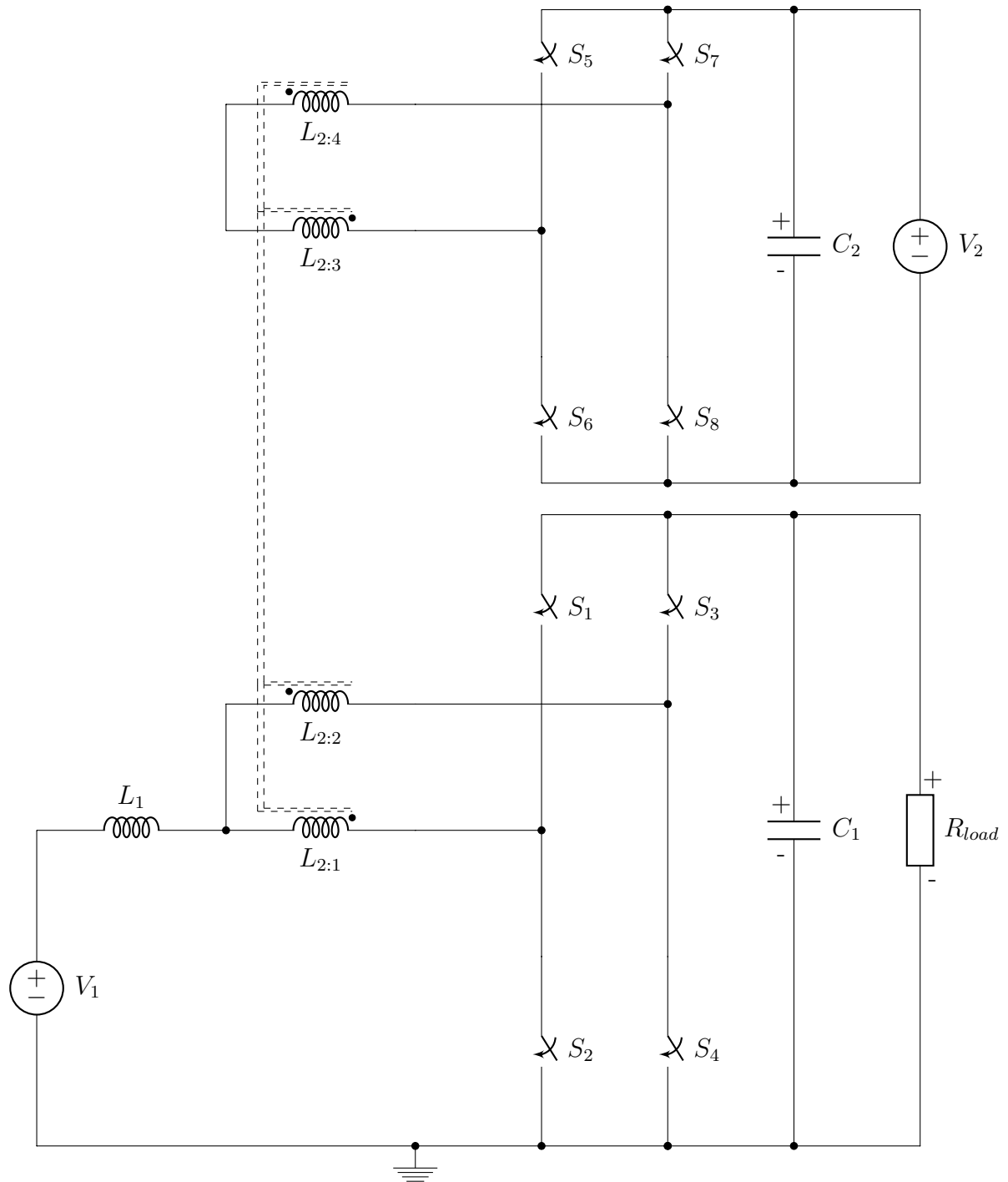


Fig. 1.38: 3SSC based isolated bidirectional soft switching converter [85–87]

In all the proposed 3SSC based converters many switches and/or diodes and/or capacitors are required to produce the voltage boost. For multiphase and coupled-multiphase topologies the amount of switches involved rises by 2-4 with each additional phase. In high current applications there may need to be many phases thus there will be 2-4 times that amount of switches needed. Conversely, in the voltage multiplier topologies the number of diodes and capacitors involved can grow rapidly depending on the required boost although this can be reduced by incorporating secondary coils with a step-up turns ratio. This added complexity provides increased opportunity for circuit losses and component failure which will reduce circuit efficiency and robustness in high power applications. Low-loss components would need to be employed to increase efficiency and robustness which will raise costs.

One common feature of all the proposed topologies covered in this section is the use of extra components to achieve higher boost ratios and/or reduce losses through various methods. While coupled inductors have become a popular feature for many recent topologies, they have mainly been accompanied by additional circuitry such as voltage multiplier circuits [41, 60–63] and storage capacitors [30, 37, 47, 64, 65, 65]. In Section 1.0.12 a new approach is explored where focussing on the coupled coils and magnetic assembly is used to achieve a simple and efficient converter.

1.0.12 The Weinberg Converter

One outstanding DC-DC converter topology was developed in 1974 by A.H. Weinberg [1]. It was intended for space applications, specifically power supply regulation in satellites. It was a step forward not only in satellite power regulation but in DC-DC converter technology in general because of its simplicity. It became very widely known as simply the “Weinberg Converter” or “Weinberg Topology” in subsequent publications throughout the years [2–9].

In space applications all power is supplied from solar-array sources and stored in batteries. This automatically applies limitations to the quantity of power available to the system and high efficiency is paramount as losses incurred in power conversion and transmission become significant and costly. Weight is also an expensive factor in space applications which is another reason why components are best kept to an absolute minimum.

Satellite and solar-array technology has evolved and improved over the years and the demands have increased. Satellite telecommunications platforms required power supplies of around 14-20kW back in 2005 and have expanded to 25kW over subsequent years [10]. This means more power being transferred from source to battery and battery to load in satellite systems.

The Weinberg converter aims to achieve a stable regulated output with high efficiency while keeping semiconductor utilisation to a minimum. For this an entirely new energy transfer principle was developed [1] where coupled magnetic systems are responsible for power transfer and switching components are simply present to provide the required excitation.

The classic Weinberg topology is shown in Figure 1.39.

The turns ratio N is given as

$$\frac{L_{1:1} + L_{1:2}}{L_{1:1}} = \frac{L_{2:1}}{L_{2:2}} = \frac{L_{3:1}}{L_{3:2}} = N$$

and the boost ratio is given by

$$\frac{V_o}{V_i} = \frac{N + 1}{N}$$

giving a maximum boost ratio of 2x which decreases as N increases; plotted in Figure 1.40.

For the intended application, output stability and efficiency are the primary objectives as the circuit is operating at high power; >500W. Here step-up is not necessary and so is not a design factor. However the inherent efficiency of the topology makes it an attractive candidate for investigation. If it can be adapted for high boost operation it could significantly enhance the performance and cost of renewable energy interfacing to systems in excess of 100VDC such as Micro-Inverters for solar panels and regenerative braking for Electric Vehicles.

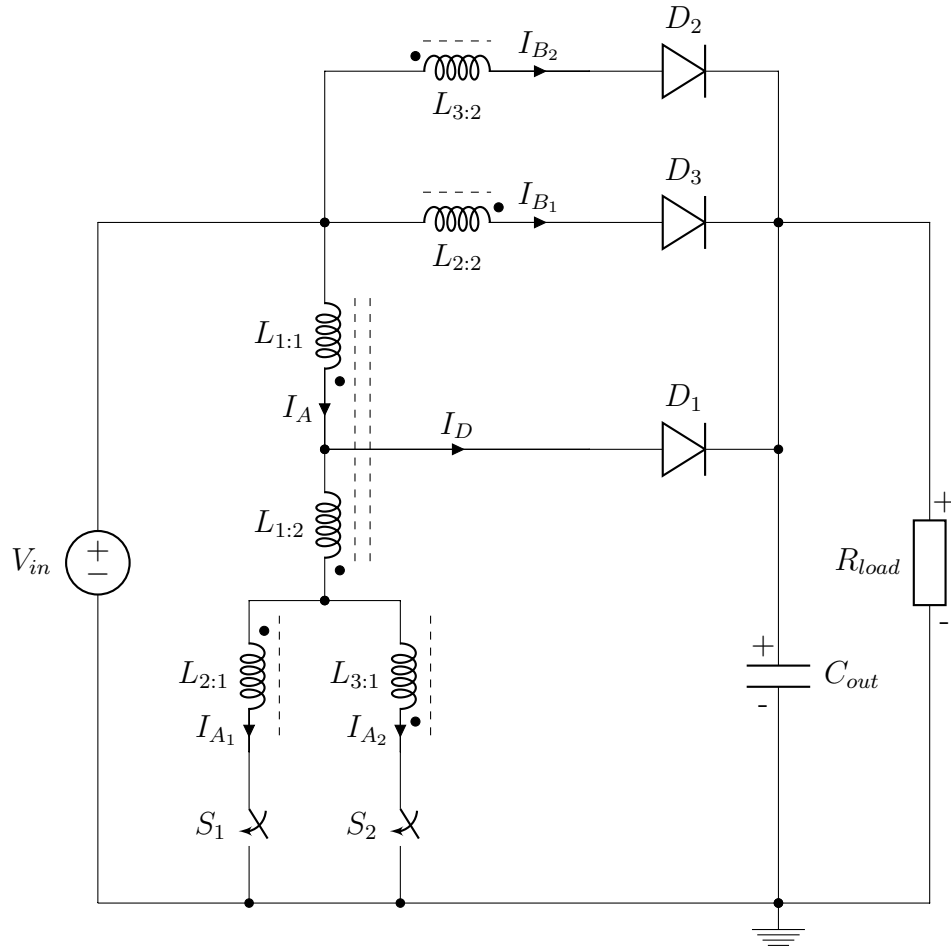


Fig. 1.39: Original Weinberg topology [1]

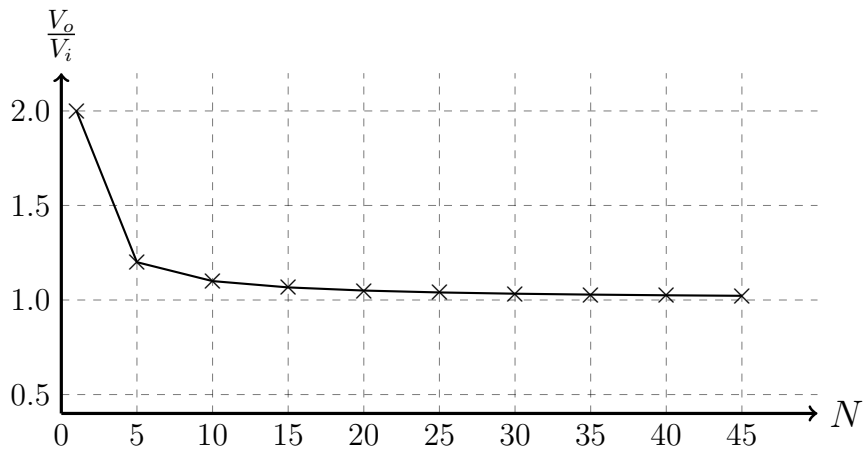


Fig. 1.40: Classic Weinberg converter boost ratio vs turns ratio [1]

A development circuit with some brief notes was also proposed in [1] shown in Figure 1.41. It would appear from the comments that the intention was to reduce switching component stresses with no implications made towards using the circuit for boosting and no transfer function provided. In subsequent decades there have been adaptations to the classic Weinberg converter [2–5, 9] with one most prominent being [2] where this development topology (Figure 1.41) is explored further for use in satellites at high power throughput. Here the topology is developed to achieve an efficiency of $>95\%$ at power throughputs of 500-1000W. The boost ratio is still 2x maximum and incorporates snubbing to achieve optimal results.

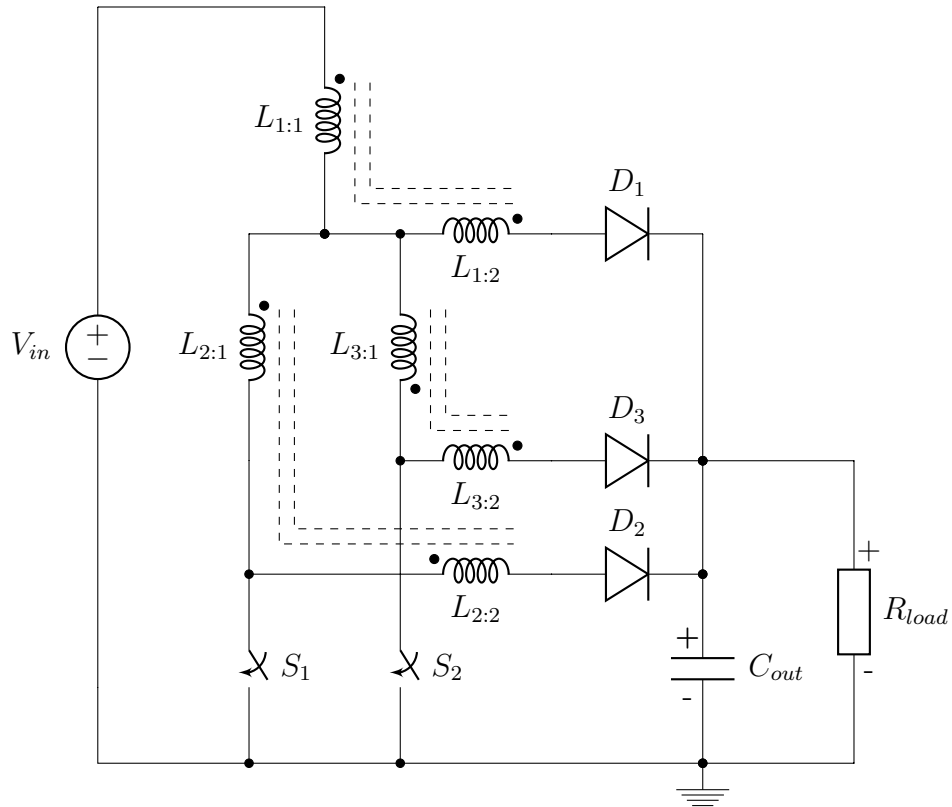


Fig. 1.41: Weinberg further development topology [1, 2]

This review has briefly outlined the evolution of DC-DC boost converters over the past fifty years. Most topologies proposed in this time follow a similar line of development resulting in many parallels and similarities emerging between them, such as the use of coupled coils to achieve higher voltage boosts. The review also shows that there has been a shift towards the use of coupled coils in DC-DC converters over recent years. All proposed topologies achieve acceptable performance, many with efficiencies well over 90% but also incorporate some shortfalls including reliance on snubbing leading to component-heavy topologies. While optimised snubbing can produce stable operation and high efficiency, it still adds to the component count leading to an increased chance of failure. In some applications reliability is more important than optimal efficiency when uninterrupted supply is paramount and access for maintenance is very difficult if not impossible.

The Weinberg converter uses the principle of energy transfer in the magnetic coils to achieve minimal external components. The coupled coils clamp the switch component voltages allowing lower breakdown voltage versions to be used. While its simplicity would tend to make it inherently reliable it has a limitation of 2x boost ratio which makes it unsuitable for many modern day applications.

2. NOVEL ADAPTABLE BOOST CONVERTER

This section introduces a novel topology based on A.H. Weinberg's suggested development from his 1974 publication [1]. It would appear that no significant investigation has been carried out on adapting the Weinberg topology for high boost operation so far as could be ascertained. The Weinberg converter uses the principle of energy transfer in the magnetic coils to achieve minimal external components but has a limitation of 2x maximum boost ratio making it unsuitable for many modern day applications. Some renewable energy sources, such as solar panels, produce output voltages of no more than about 45VDC. For supplying Grid-Tie or electric vehicle battery charging systems require voltages to be boosted to above 200VDC in many cases.

A novel topology is developed in this section which preserves most of the features of the Weinberg design and adapts it to achieve high-boosting capability.

LTSpice is a widely employed simulation tool and is used to verify mathematical analysis performed in this section.

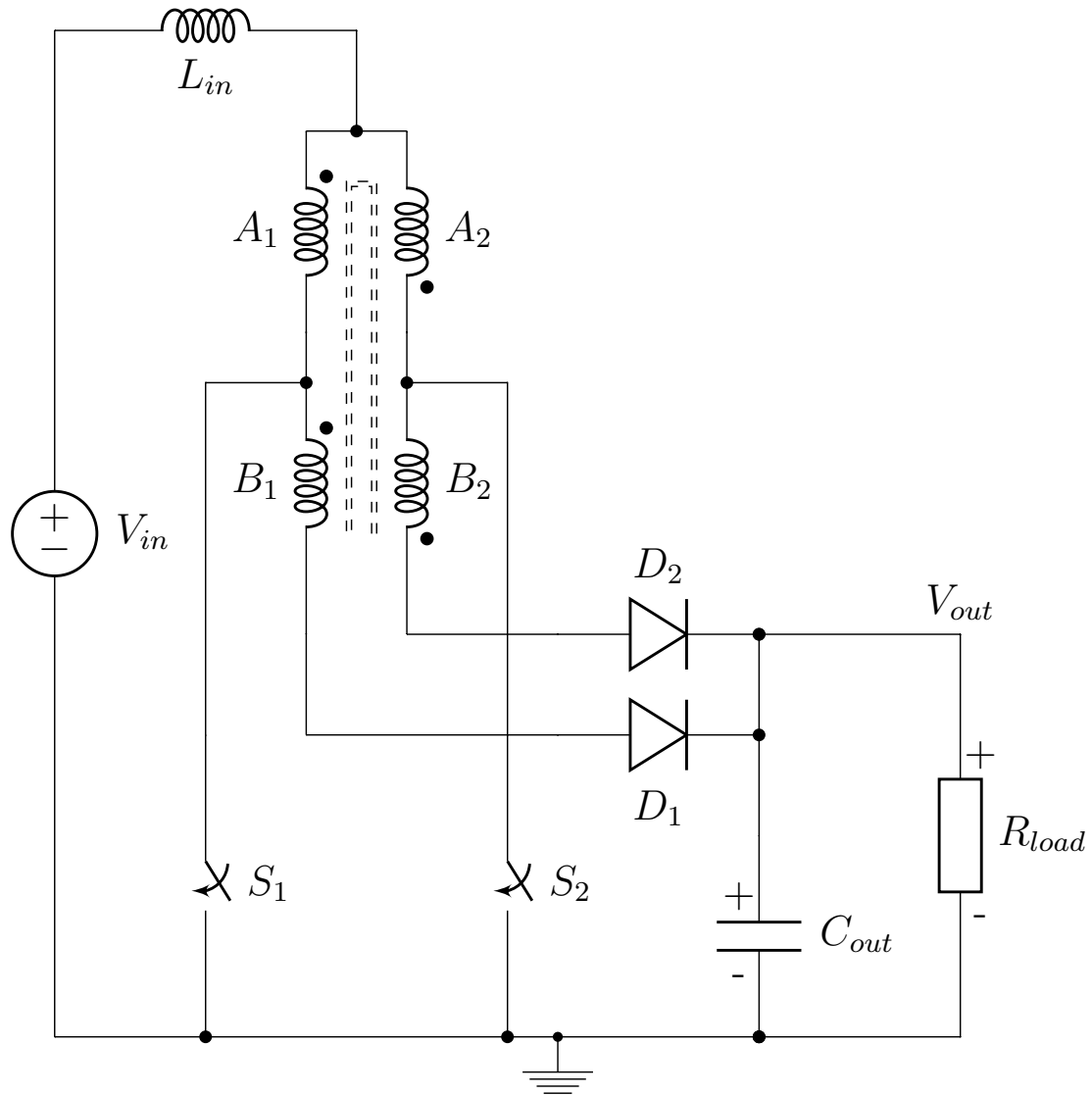


Fig. 2.1: Proposed Topology

2.0.1 Analysis of the Proposed Topology

An analysis of the novel topology is performed in this Section. In Section 2.0.2 the circuit is modelled with a varying output voltage and the voltage transfer function is derived. In Section 2.0.3 the circuit is modelled with a constant output voltage and a current analysis is carried out.

The voltage and current for an inductor are related by

$$V_L = L \frac{\Delta i_L}{\Delta t} \quad (2.1)$$

Any two inductors wound on a common core will influence each others' voltage. If two inductors L_1 and L_2 share a common core then they will have a mutual inductance M . The overall voltage will be reinforced or cancelled depending on the phase alignments of the two coils involved.

$$V_{L_1} = L_1 \frac{\Delta i_{L_1}}{\Delta t} \pm M \frac{\Delta i_{L_2}}{\Delta t} \quad (2.2)$$

$$V_{L_2} = L_2 \frac{\Delta i_{L_2}}{\Delta t} \pm M \frac{\Delta i_{L_1}}{\Delta t} \quad (2.3)$$

$$M = \sqrt{L_1 L_2} \quad (2.4)$$

2.0.2 Unregulated Output Voltage Analysis

Most basic loads do not control their voltage, a voltage is applied to them by the power supply circuitry. If an unregulated voltage load such as this is attached to the output of a DC-DC converter, the output of the converter circuit sets the applied voltage to the load. The circuit operates under its voltage transfer function and is responsible for regulating the load voltage if required. This section outlines the basic derivation of the voltage transfer function for the circuit.

The input current waveform is shown in Figure 2.6 along with its timing labels. The proposed circuit has two main states of operation. The first when both switches are closed (Figure 2.2) termed the "Overlap Period" and denoted mathematically as $t_{(OV)}$ in Figure 2.6. The second when only one switch is closed and the other is open (Figure 2.3) termed the "Non-Overlap Period" and from Figure 2.6 this can be denoted mathematically as $(\frac{T}{2} - t_{(OV)})$. Both primary and both secondary windings have equal inductance so their terminology can be generalised to

$$L_{A_1} = L_{A_2} = L_A \quad (2.5)$$

$$L_{B_1} = L_{B_2} = L_B \quad (2.6)$$

$$V_{A_1} = V_{A_2} = V_A \quad (2.7)$$

$$V_{B_1} = V_{B_2} = V_B \quad (2.8)$$

The duty cycle is defined in this analysis as the ratio of the overlap time to the full switching period

$$D = \frac{t_{(ov)}}{t_{(ov)} + \left(\frac{T}{2} - t_{(ov)}\right)} = 2 \frac{t_{(ov)}}{T} \quad (2.9)$$

The transfer function can be derived by analysing the two operating states.

Both Switches Closed ($t_{(ov)}$)

With both switches closed the node voltage V_N as shown in Figure 2.2 is virtual ground (see Section 2.0.3)

$$V_N = 0$$

thus the potential difference across L_{in} is given from (2.1) as

$$V_{L_{in}} = V_{in} - V_N = L_{in} \frac{\Delta i_{in}}{t_{(ov)}}$$

where $V_N = 0$ and applying (2.9) gives

$$V_{in} = 2L_{in} \frac{\Delta i_{in}}{DT} \quad (2.10)$$

In steady state operation Δi_{in} has an equal value for both modes of operation. Therefore rearrange (2.10) to give

$$\Delta i_{in} = \frac{V_{in}DT}{2L_{in}} \quad (2.11)$$

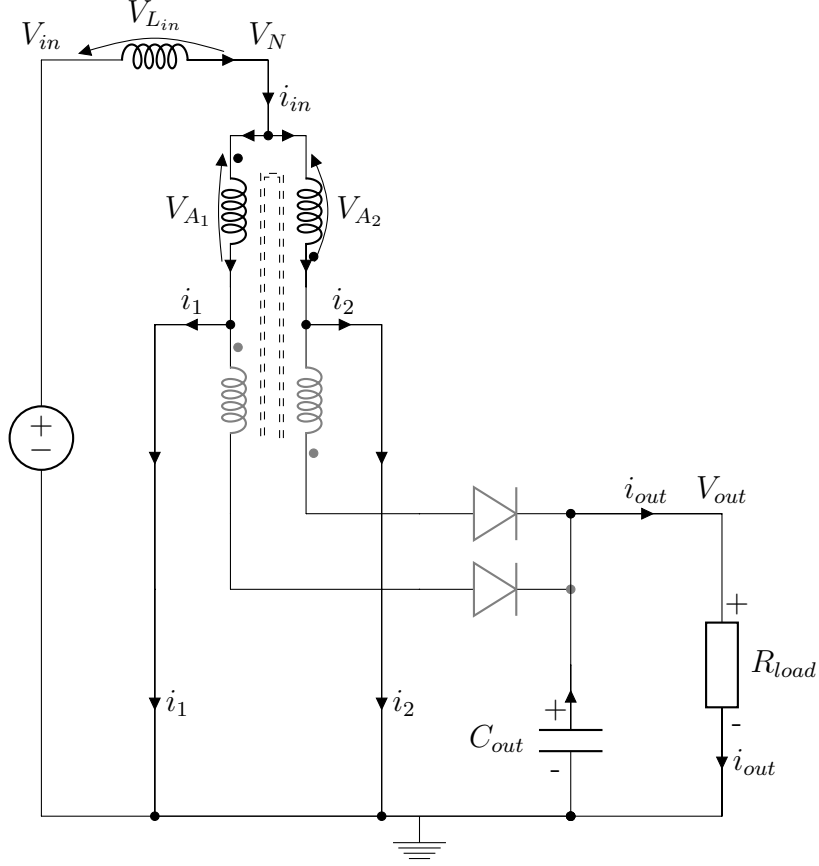


Fig. 2.2: Mode 1: Both Switches Closed

One Switch Closed $\left(\frac{T}{2} - t_{(OV)}\right)$

During this period, as shown in Figure 2.3, the potential difference across L_{in} is given from (2.1) as

$$V_{L_{in}} = V_{in} - V_N = -L_{in} \frac{\Delta i_{in}}{\left(\frac{T}{2} - t_{(OV)}\right)}$$

$$-(V_{in} - V_N) = L_{in} \frac{\Delta i_{in}}{\left(\frac{T}{2} - t_{(OV)}\right)}$$

applying (2.9)

$$V_N - V_{in} = L_{in} \frac{\Delta i_{in}}{\left(\frac{T}{2} - D\frac{T}{2}\right)}$$

$$V_N - V_{in} = L_{in} \frac{\Delta i_{in}}{\frac{T}{2} (1 - D)}$$

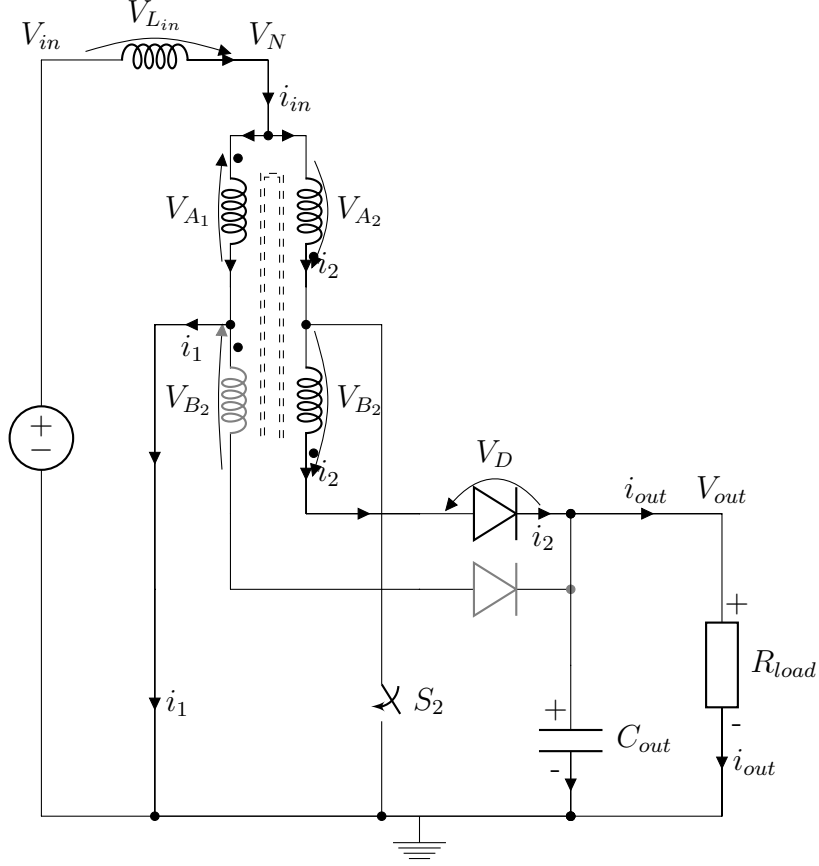


Fig. 2.3: Mode 2: One Switch Closed

$$\begin{aligned}
 V_N - V_{in} &= 2L_{in} \frac{\Delta i_{in}}{T(1-D)} \\
 \Delta i_{in} &= \frac{(V_N - V_{in}) T(1-D)}{2L_{in}}
 \end{aligned} \tag{2.12}$$

For the purpose of this model let

$$\frac{V_B}{V_A} = \sqrt{\frac{L_B}{L_A}} = \eta \tag{2.13}$$

From Figure 2.3 the output voltage is the sum of the three active transformer winding voltages

$$V_{out} = V_{A1} + V_{A2} + V_{B2} = 2V_A + V_B$$

where

$$V_N = V_A$$

Applying (2.13)

$$\begin{aligned} V_{out} &= 2V_A + V_A\eta \\ V_{out} &= V_A(2 + \eta) \\ V_N &= V_A = \frac{V_{out}}{2 + \eta} \end{aligned} \quad (2.14)$$

Applying to (2.12) gives

$$\Delta i_{L_{in}} = \frac{\left(\frac{V_{out}}{2+\eta} - V_{in}\right)(1-D)T}{2L_{in}} \quad (2.15)$$

During steady state operation i_{in} rises and falls by equal amounts from its maximum to its minimum values meaning the magnitudes of (2.11) and (2.15) can be equated to give

$$\begin{aligned} \frac{V_{in}DT}{2L_{in}} &= \Delta i_{L_{in}} = \frac{\left(\frac{V_{out}}{2+\eta} - V_{in}\right)(1-D)T}{2L_{in}} \\ V_{in}D &= \left(\frac{V_{out}}{2+\eta} - V_{in}\right)(1-D) \\ V_{in}D &= \frac{V_{out}}{2+\eta} - V_{in} - \frac{V_{out}}{2+\eta}D + V_{in}D \\ V_{in}D - V_{in}D + V_{in} &= \frac{V_{out}}{2+\eta} - \frac{V_{out}}{2+\eta}D \\ V_{in} &= \frac{V_{out}}{2+\eta}(1-D) \\ \frac{V_{in}}{V_{out}} &= \frac{1-D}{2+\eta} \end{aligned}$$

giving a final voltage transfer function of

$$\frac{V_{out}}{V_{in}} = (2 + \eta) \left(\frac{1}{1-D} \right) \quad (2.16)$$

This transfer function comprises both the basic boost transfer function $\left(\frac{1}{1-D}\right)$, and a scaling factor of $(2 + \eta)$ governed by the turns ratio of the transformer windings. From Figure 2.3 the maximum blocking potential difference across the controlled switches is $2V_A$ and the maximum blocking potential across the diode is $V_{out} + V_B$. These are quantified in Section 2.0.3. This enables the choice of appropriate components, and also leads to the controlled switches having a lower blocking potential compared to the diodes, permitting the use of devices with high current capability and lower intrinsic resistance.

2.0.3 Regulated Output Voltage Analysis

In applications such as battery charging or grid-tie, the load is a battery or a power system. These produce and can also regulate their own voltage. If a regulated voltage load such as this is attached to the output of a DC-DC converter, the converter no longer controls the output voltage. This means the voltage transfer function, as derived in Section 2.0.2, no longer applies. Instead the circuit regulates the current flow, and hence the power throughput, which is analysed under ideal conditions in this section.

An equivalent layout of the proposed topology is shown in Figure 2.4. Switches S_1 and S_2 and forward conducting diodes D_1 and D_2 are modelled as ideal components. For the switches this means open circuit when open ($R_{off} = \infty\Omega$) and short circuit when closed ($R_{on} = 0\Omega$) with instantaneous transitions between states. For the diodes this means short circuit when forward biased and open circuit when reverse biased with instantaneous transitions between states.

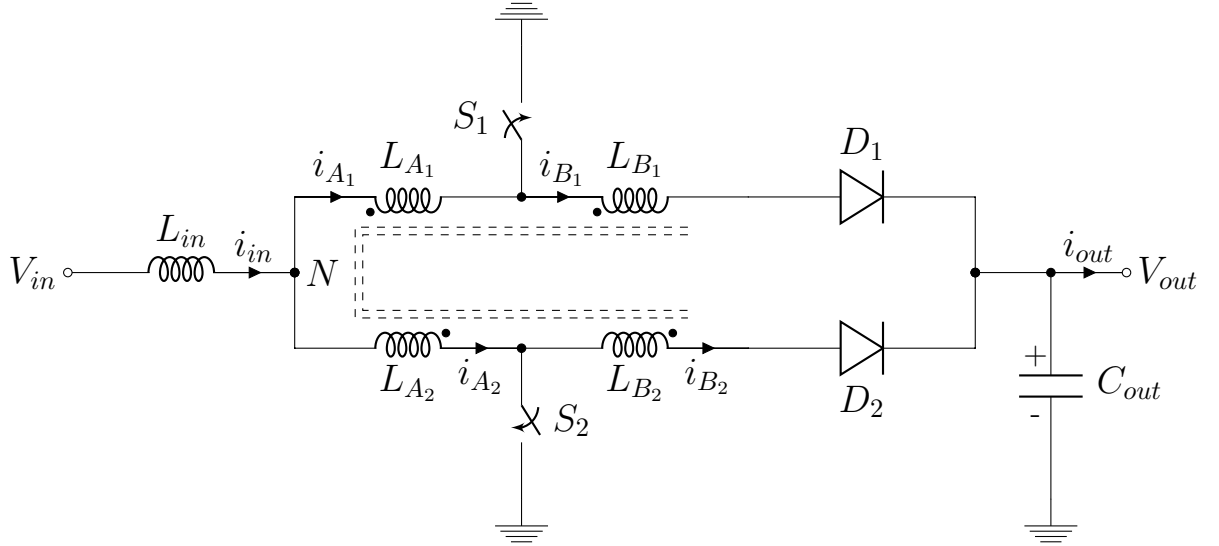


Fig. 2.4: Equivalent representation of the proposed topology

The two switches S_1 and S_2 have a switching period T and are offset in time by $\frac{T}{2}$. For each half-period $\frac{T}{2}$ there is one state where both switches are closed and two states where only one switch is closed. These repeat twice throughout an entire switching period T because of the dual-switch topology. The period where both switches are closed is termed the “Overlap Period” and denoted as $t_{(ov)}$ in Figure 2.5, 2.6.

The current waveforms through all coils over a complete switching period T are shown in Figure 2.5. The input current i_{in} rises from a minimum value $i_{in(min)}$

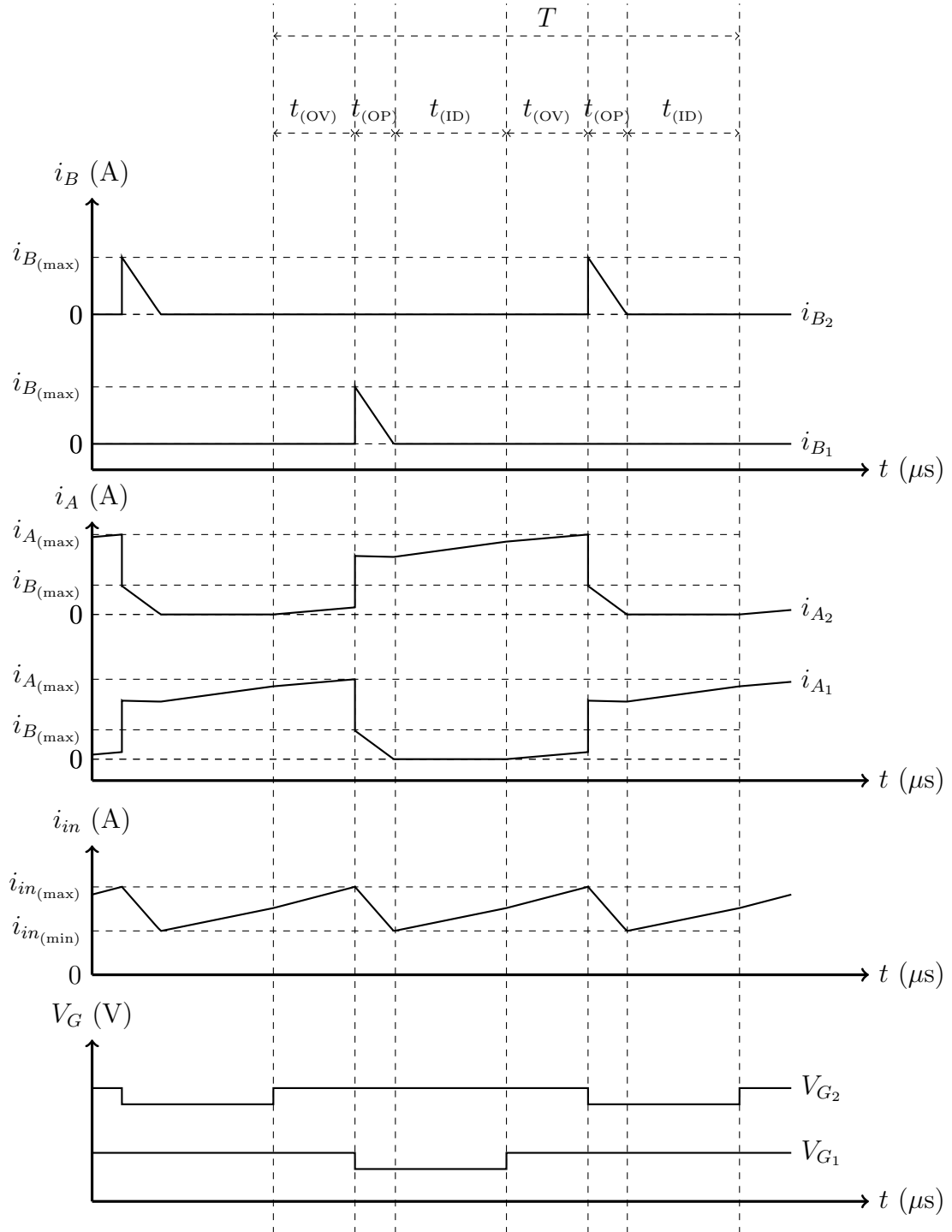


Fig. 2.5: Current waveforms for all coils shown in Figure 2.4 using simulation data

to a maximum value $i_{in(max)}$ and back again over time $\frac{T}{2}$ as shown in Figure 2.6. Due to the overlap the effective switching period of the two switches combined is $\frac{T}{2}$. The duty cycle is defined in this analysis as the ratio of the overlap time to the full switching period

$$D = \frac{t_{(OV)}}{t_{(OV)} + t_{(OP)} + t_{(ID)}} = \frac{2t_{(OV)}}{T} \quad (2.17)$$

An analysis of the circuit behavior over these periods is presented in this section.

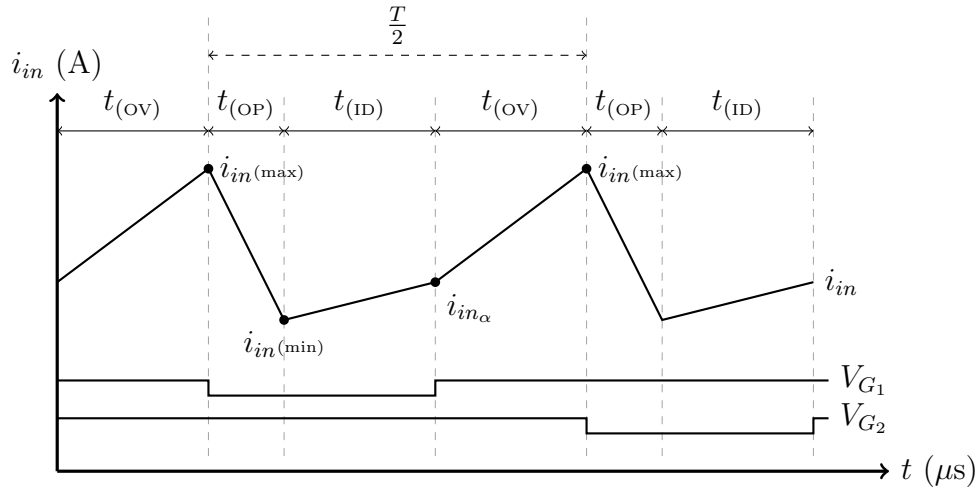


Fig. 2.6: Expanded input current waveform

V_{G1} , V_{G2} represent the voltage signals applied to the MOSFET gates.

Unlike regular single-switch converters the rise and fall of the input inductor current i_{in} is not simply related to these switching times. If it is assumed that the rise and fall times of i_{in} are completely dependent on the switching times the calculation produces a result with unrelated trend to the simulation as shown in Figure 2.7.

Equations are derived which correctly quantify the average input current for a given set of switching parameters, this is where the two traces in Figure 2.7 intersect. However when the switching parameters are adjusted the simulation and calculation produce completely divergent outputs. The circuit “Self-Commutates” meaning when the energy stored in inductor L_{in} falls below the amount needed to generate the output voltage the circuit automatically begins recharging it without intervention from the switching. This is made possible because there are two switches and at least one is always closed meaning there is never a situation where no current path exists through L_{in} . As a result the recharging of the inductor is not dependent on the open switch closing and hence not dependent on the switch

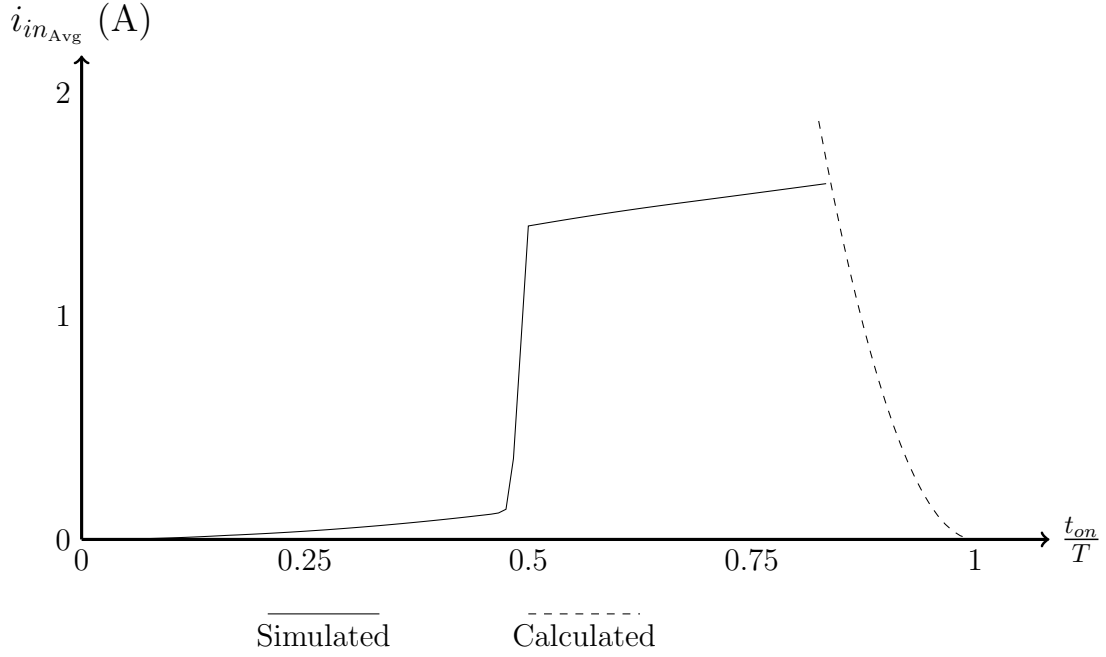


Fig. 2.7: Calculated vs simulated input current against switch-on time assuming complete dependence on switching

For each switch, t_{on} represents the time within a switch period T for which that switch is closed. Circuit is in discontinuous current operation when $\frac{t_{on}}{T} < 0.5$

timing. If the switch on-time t_{on} becomes less than a half-period ($\frac{t_{on}}{T} < 0.5$) then there is a time period where no current path exists through L_{in} . The current through L_{in} reduces to zero during this period and the circuit enters discontinuous current mode.

The voltage at the node labelled N in Figure 2.4 changes over time. The expanded current and voltage waveforms for the transformer are shown in Figure 2.8 which illustrates how V_N varies over the switching period T . The value of V_N during the time periods $t_{(OV)}$, $t_{(OP)}$, $t_{(ID)}$ are labelled as $V_{N(OV)}$, $V_{N(OP)}$, $V_{N(ID)}$ respectively in the derivation.

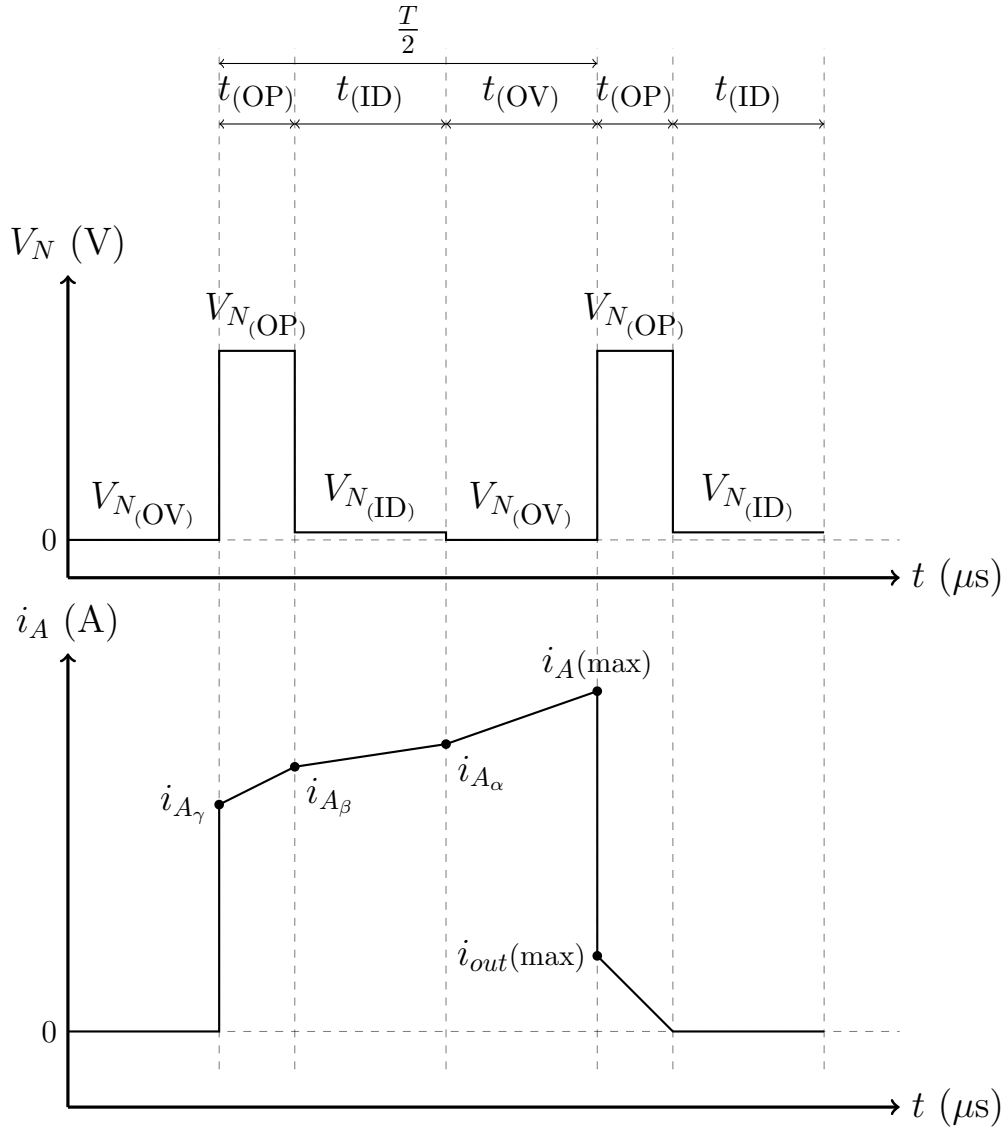


Fig. 2.8: Expanded transformer current and voltage waveforms showing the node voltage V_N and primary coil current i_A over a switching period T

For this analysis it can be assumed that the following conditions are always true

$$L_{A1} = L_{A2} = L_A \quad (2.18)$$

$$L_{B1} = L_{B2} = L_B \quad (2.19)$$

$$V_{A1} = V_{A2} = V_A \quad (2.20)$$

$$V_{B1} = V_{B2} = V_B \quad (2.21)$$

$$\eta = \sqrt{\frac{L_B}{L_A}} = \frac{V_B}{V_A} \quad (2.22)$$

$$i_{in} = i_{A1} + i_{A2} \quad (2.23)$$

$$\frac{\Delta i_{in}}{\Delta t} = \frac{\Delta i_{A1}}{\Delta t} + \frac{\Delta i_{A2}}{\Delta t} \quad (2.24)$$

$$i_{out} = i_{B1} + i_{B2} \quad (2.25)$$

The equivalent circuit during the overlap period is shown in Figure 2.9.

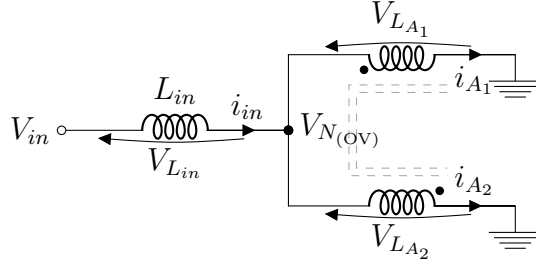


Fig. 2.9: Equivalent circuit during overlap period $t_{(ov)}$

Using (2.2)(2.3) the combined inductance of the transformer in this state can be determined as

$$V_{N(ov)} = V_{A1} = L_A \frac{\Delta i_{A1}}{t_{(ov)}} - M_{A1A2} \frac{\Delta i_{A2}}{t_{(ov)}} \quad (2.26)$$

$$V_{N(ov)} = V_{A2} = L_A \frac{\Delta i_{A2}}{t_{(ov)}} - M_{A1A2} \frac{\Delta i_{A1}}{t_{(ov)}} \quad (2.27)$$

$$M_{A1A2} = \sqrt{L_A L_A} = \sqrt{L_A^2} = L_A \quad (2.28)$$

equating (2.26) and (2.27) gives

$$L_A \frac{\Delta i_{A1}}{t_{(ov)}} - M_{A1A2} \frac{\Delta i_{A2}}{t_{(ov)}} = L_A \frac{\Delta i_{A2}}{t_{(ov)}} - M_{A1A2} \frac{\Delta i_{A1}}{t_{(ov)}}$$

substituting (2.28)

$$\begin{aligned} L_A \frac{\Delta i_{A1}}{t_{(OV)}} - L_A \frac{\Delta i_{A2}}{t_{(OV)}} &= L_A \frac{\Delta i_{A2}}{t_{(OV)}} - L_A \frac{\Delta i_{A1}}{t_{(OV)}} \\ (L_A + L_A) \frac{\Delta i_{A1}}{t_{(OV)}} &= (L_A + L_A) \frac{\Delta i_{A2}}{t_{(OV)}} \\ 2L_A \frac{\Delta i_{A1}}{t_{(OV)}} &= 2L_A \frac{\Delta i_{A2}}{t_{(OV)}} \end{aligned}$$

which finally gives

$$\frac{\Delta i_{A1}}{t_{(OV)}} = \frac{\Delta i_{A2}}{t_{(OV)}} \quad (2.29)$$

L_{A1} and L_{A2} are anti-phase in this state. If the current gradients are equal as shown by (2.29) then their voltages cancel meaning

$$V_{N(OV)} = 0 \quad (2.30)$$

In Figure 2.9 the voltage across inductor L_{in} can be determined from (2.1) as

$$V_{L_{in}} = V_{in} - V_{N(OV)} = L_{in} \frac{\Delta i_{in(OV)}}{t_{(OV)}}$$

with $V_{N(OV)} = 0$ this rearranges to give

$$\Delta i_{in(OV)} = \frac{V_{in}}{L_{in}} t_{(OV)}$$

substituting (2.17)

$$\Delta i_{in(OV)} = i_{in(max)} - i_{in\alpha} = \frac{V_{in}}{L_{in}} D \frac{T}{2} \quad (2.31)$$

When either switch opens the circuit enters its outputting period, denoted as $t_{(OP)}$. The equivalent circuit schematic with S_1 open is shown in Figure 2.10.

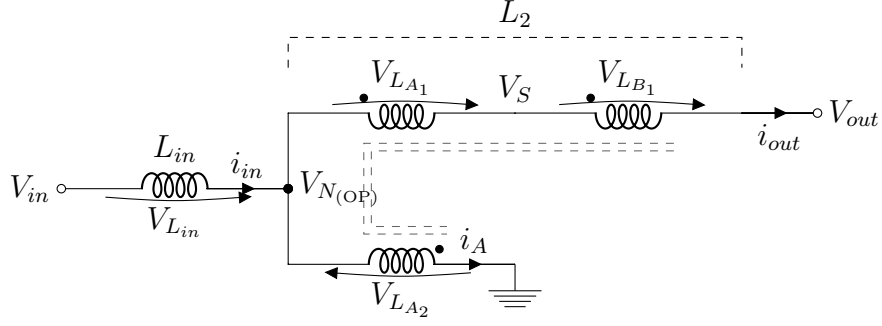


Fig. 2.10: Equivalent circuit during output period $t_{(OP)}$ with S_1 open

The change in input current over period $t_{(OP)}$ is negative. The voltage across L_{in} can be determined from (2.1) as

$$V_{in} - V_{N(OP)} = -L_{in} \frac{\Delta i_{in(OP)}}{t_{(OP)}}$$

$$-(V_{in} - V_{N(OP)}) = L_{in} \frac{\Delta i_{in(OP)}}{t_{(OP)}}$$

$$V_{N(OP)} - V_{in} = L_{in} \frac{\Delta i_{in(OP)}}{t_{(OP)}}$$

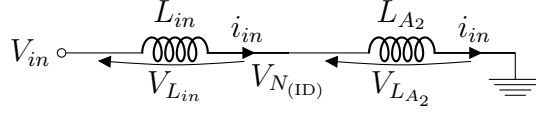
from (2.14)

$$V_{N(OP)} = \frac{V_{out}}{2 + \eta}$$

$$\frac{V_{out}}{2 + \eta} - V_{in} = L_{in} \frac{\Delta i_{in(OP)}}{t_{(OP)}}$$

$$\Delta i_{in(OP)} = i_{in(max)} - i_{in(min)} = \left(\frac{V_{out}}{2 + \eta} - V_{in} \right) \frac{t_{(OP)}}{L_{in}} \quad (2.32)$$

The energy which produces the voltage boost is sourced from L_{in} . When the energy stored in L_{in} drops below that required to generate voltage higher than V_{out} the forward conducting diode D_1 stops conducting and cuts off the current path. The entire transformer arrangement is now out of circuit as there are no current paths. Only L_{A2} remains in circuit but will act as a normal inductor due to the rest of the transformer conducting zero current. The equivalent circuit is shown in Figure 2.11.

Fig. 2.11: Equivalent circuit during free-wheeling period $t_{(ID)}$

Applying (2.1)

$$V_{N(ID)} = L_A \frac{\Delta i_{in(ID)}}{t_{(ID)}} \quad (2.33)$$

$$V_{in} - V_{N(ID)} = L_{in} \frac{\Delta i_{in(ID)}}{t_{(ID)}} \quad (2.34)$$

Adding (2.33) and (2.34)

$$V_{in} = L_A \frac{\Delta i_{in(ID)}}{t_{(ID)}} + L_{in} \frac{\Delta i_{in(ID)}}{t_{(ID)}}$$

$$V_{in} = (L_{in} + L_A) \frac{\Delta i_{in(ID)}}{t_{(ID)}}$$

$$\Delta i_{in(ID)} = \frac{V_{in}}{L_{in} + L_A} t_{(ID)}$$

from (2.17)

$$t_{(ID)} = \frac{T}{2} - t_{(OV)} - t_{(OP)}$$

$$t_{(OV)} = D \frac{T}{2}$$

$$t_{(ID)} = \frac{T}{2} - D \frac{T}{2} - t_{(OP)}$$

$$\Delta i_{in(ID)} = i_{in\alpha} - i_{in(\min)} = \frac{V_{in}}{L_{in} + L_A} \left[\frac{T}{2} (1 - D) - t_{(OP)} \right] \quad (2.35)$$

Output Conduction Time

Δi_{in} over all three switching states defined in Figure 2.6 are now quantified in terms of $t_{(OP)}$. Apply (2.23)

$$\Delta i_{in(OP)} = \Delta i_{in(OV)} + \Delta i_{in(ID)}$$

and substitute (2.31), (2.32), (2.35) to give

$$\begin{aligned}
 \left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{t_{(OP)}}{L_{in}} &= \frac{V_{in}}{L_{in}} D \frac{T}{2} + \frac{V_{in}}{L_{in} + L_A} \left[\frac{T}{2} (1-D) - t_{(OP)} \right] \\
 \left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{t_{(OP)}}{L_{in}} &= \frac{V_{in}}{L_{in}} D \frac{T}{2} + \frac{V_{in}}{L_{in} + L_A} \frac{T}{2} (1-D) - \frac{V_{in}}{L_{in} + L_A} t_{(OP)} \\
 \left[\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in} + L_A} \right] t_{(OP)} &= \frac{V_{in}}{L_{in}} D \frac{T}{2} + \frac{V_{in}}{L_{in} + L_A} \frac{T}{2} (1-D) \\
 t_{(OP)} &= \frac{\frac{V_{in}}{L_{in}} D \frac{T}{2} + \frac{V_{in}}{L_{in} + L_A} \frac{T}{2} (1-D)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in} + L_A}} \\
 t_{(OP)} &= \frac{\frac{V_{in} T}{2} \left(\frac{D}{L_{in}} + \frac{1-D}{L_{in} + L_A} \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in} + L_A}}
 \end{aligned}$$

Simplify the numerator fractions by cross-multiplying

$$t_{(OP)} = \frac{\frac{V_{in} T}{2} \left(\frac{(L_{in} + L_A) D + L_{in} (1-D)}{L_{in}^2 + L_{in} L_A} \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in} + L_A}}$$

expand the numerator brackets

$$t_{(OP)} = \frac{\frac{V_{in} T}{2} \left(\frac{L_{in} D + L_A D + L_{in} - L_{in} D}{L_{in}^2 + L_{in} L_A} \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in} + L_A}}$$

simplify numerator expressions

$$t_{(OP)} = \frac{\frac{V_{in} T}{2} \left(\frac{L_A D + L_{in}}{L_{in}^2 + L_{in} L_A} \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in} + L_A}}$$

separate into two separate fractions with common denominator

$$t_{(OP)} = \frac{\frac{V_{in} T}{2} \left(\frac{L_A D}{L_{in}^2 + L_{in} L_A} + \frac{L_{in}}{L_{in}^2 + L_{in} L_A} \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in} + L_A}}$$

simplify denominator

$$t_{(OP)} = \frac{\frac{V_{in} T}{2} \left(\frac{L_A D}{(L_{in} + L_A) L_{in}} + \frac{L_{in}}{(L_{in} + L_A) L_{in}} \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in} + L_A}}$$

final simplification, extract common denominator

$$t_{(\text{OP})} = T \frac{\frac{V_{in}}{2(L_{in}+L_A)} \left(D \frac{L_A}{L_{in}} + 1 \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in}+L_A}} \quad (2.36)$$

Assuming that D and V_{out} are constant, (2.36) quantifies $t_{(\text{OP})}$ from static circuit parameters and only one settable parameter T . This allows all terms dependent on $t_{(\text{OP})}$ to be quantified.

Average Output Current

During $t_{(\text{OP})}$ there are two transformer coils L_{A1}, L_{B1} sharing a common current. Using (2.2), (2.3) their combined inductance can be derived as

$$V_{L_B} = V_{out} - V_S = L_B \frac{\Delta i_{out}}{t_{(\text{OP})}} + M_{AB} \frac{\Delta i_{out}}{t_{(\text{OP})}} \quad (2.37)$$

$$V_{L_A} = V_S - V_{N(\text{OP})} = L_A \frac{\Delta i_{out}}{t_{(\text{OP})}} + M_{AB} \frac{\Delta i_{out}}{t_{(\text{OP})}} \quad (2.38)$$

$$M_{AB} = \sqrt{L_A L_B} \quad (2.39)$$

the combined voltage is determined by adding (2.37) and (2.38)

$$V_{out} - V_{N(\text{OP})} = L_B \frac{\Delta i_{out}}{t_{(\text{OP})}} + M_{AB} \frac{\Delta i_{out}}{t_{(\text{OP})}} + L_A \frac{\Delta i_{out}}{t_{(\text{OP})}} + M_{AB} \frac{\Delta i_{out}}{t_{(\text{OP})}}$$

$$V_{out} - V_{N(\text{OP})} = (L_A + L_B + 2M_{AB}) \frac{\Delta i_{out}}{t_{(\text{OP})}}$$

substituting (2.39)

$$V_{out} - V_{N(\text{OP})} = (L_A + L_B + 2\sqrt{L_A L_B}) \frac{\Delta i_{out}}{t_{(\text{OP})}}$$

the combined inductance is termed L_2 in Figure 2.10 so

$$V_{out} - V_{N(\text{OP})} = L_2 \frac{\Delta i_{out}}{t_{(\text{OP})}}$$

where

$$L_2 = L_A + L_B + 2\sqrt{L_A L_B} \quad (2.40)$$

All active transformer coils contribute to the output voltage during this state. This allows a larger output voltage to be generated than with just a single tapped inductor. Applying (2.2), (2.3)

$$V_{out} - V_{N(OP)} = - \left(-L_2 \frac{\Delta i_{out}}{t_{(OP)}} - M_{L_2 A} \frac{\Delta i_A}{t_{(OP)}} \right) \quad (2.41)$$

$$V_{N(OP)} = L_A \frac{\Delta i_A}{t_{(OP)}} + M_{L_2 A} \frac{\Delta i_{out}}{t_{(OP)}} \quad (2.42)$$

$$M_{L_2 A} = \sqrt{L_2 L_A} \quad (2.43)$$

substituting (2.42) into (2.41)

$$\begin{aligned} V_{out} - \left(L_A \frac{\Delta i_A}{t_{(OP)}} + M_{L_2 A} \frac{\Delta i_{out}}{t_{(OP)}} \right) &= - \left(-L_2 \frac{\Delta i_{out}}{t_{(OP)}} - M_{L_2 A} \frac{\Delta i_A}{t_{(OP)}} \right) \\ V_{out} - L_A \frac{\Delta i_A}{t_{(OP)}} - M_{L_2 A} \frac{\Delta i_{out}}{t_{(OP)}} &= L_2 \frac{\Delta i_{out}}{t_{(OP)}} + M_{L_2 A} \frac{\Delta i_A}{t_{(OP)}} \\ V_{out} &= L_2 \frac{\Delta i_{out}}{t_{(OP)}} + M_{L_2 A} \frac{\Delta i_A}{t_{(OP)}} + L_A \frac{\Delta i_A}{t_{(OP)}} + M_{L_2 A} \frac{\Delta i_{out}}{t_{(OP)}} \end{aligned}$$

Applying (2.23)

$$\begin{aligned} \Delta i_A &= -\Delta i_{in(OP)} + \Delta i_{out} \\ V_{out} &= L_2 \frac{\Delta i_{out}}{t_{(OP)}} + \frac{M_{L_2 A}}{t_{(OP)}} (-\Delta i_{in(OP)} + \Delta i_{out}) + \frac{L_A}{t_{(OP)}} (-\Delta i_{in(OP)} + \Delta i_{out}) + M_{L_2 A} \frac{\Delta i_{out}}{t_{(OP)}} \\ V_{out} &= L_2 \frac{\Delta i_{out}}{t_{(OP)}} - M_{L_2 A} \frac{\Delta i_{in(OP)}}{t_{(OP)}} + M_{L_2 A} \frac{\Delta i_{out}}{t_{(OP)}} - L_A \frac{\Delta i_{in(OP)}}{t_{(OP)}} + L_A \frac{\Delta i_{out}}{t_{(OP)}} + M_{L_2 A} \frac{\Delta i_{out}}{t_{(OP)}} \\ V_{out} &= (L_2 + 2M_{L_2 A} + L_A) \frac{\Delta i_{out}}{t_{(OP)}} + (-L_A - M_{L_2 A}) \frac{\Delta i_{in(OP)}}{t_{(OP)}} \end{aligned}$$

substituting (2.43)

$$V_{out} = \left(L_A + L_2 + 2\sqrt{L_2 L_A} \right) \frac{\Delta i_{out}}{t_{(OP)}} + \left(-L_A - \sqrt{L_2 L_A} \right) \frac{\Delta i_{in(OP)}}{t_{(OP)}}$$

giving the final solution

$$\Delta i_{out} = \frac{\left[V_{out} + (L_A + \sqrt{L_2 L_A}) \frac{\Delta i_{in(OP)}}{t_{(OP)}} \right] t_{(OP)}}{L_A + L_2 + 2\sqrt{L_2 L_A}} \quad (2.44)$$

An expanded plot of the output current is shown in Figure 2.12.

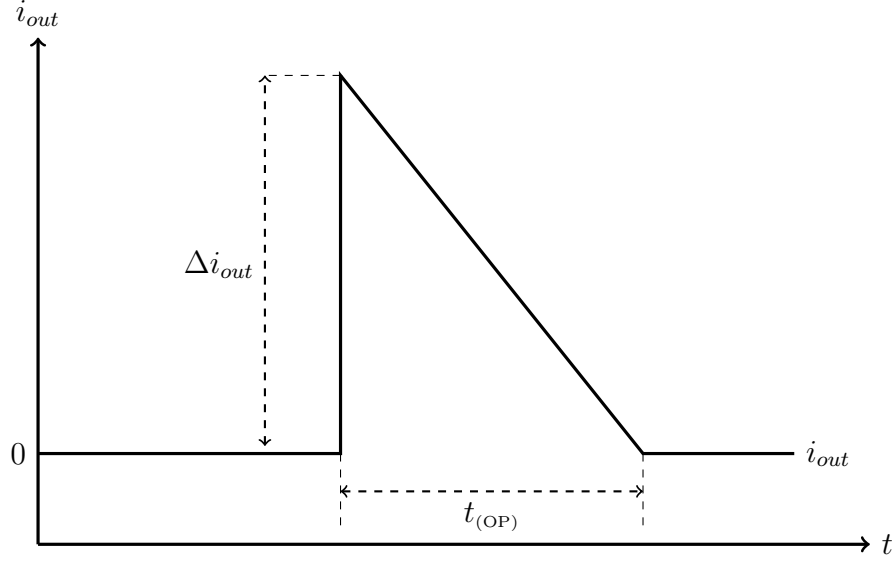


Fig. 2.12: Expanded Output current Waveform

The average output current over period $\frac{T}{2}$ is given by

$$\begin{aligned}
 i_{out(Avg)} &= \frac{2}{T} \int_0^{\frac{T}{2}} i_{out} \cdot dt \\
 i_{out(Avg)} &= \frac{2}{T} \left(\frac{1}{2} t_{(OP)} \times \Delta i_{out} \right) \\
 i_{out(Avg)} &= \frac{t_{(OP)}}{T} \Delta i_{out}
 \end{aligned} \tag{2.45}$$

Average Input Current

The input and output powers are related by

$$P_{out} = \epsilon P_{in}$$

where ϵ is the overall circuit efficiency which is assumed to be unity in this model.

$$V_{out} i_{out(Avg)} = \epsilon V_{in} i_{in(Avg)}$$

$$i_{in(Avg)} = \frac{V_{out} i_{out(Avg)}}{\epsilon V_{in}}$$

substituting (2.45) and (2.44) gives

$$i_{in(Avg)} = \frac{V_{out}}{\epsilon V_{in}} \left[\frac{t_{(OP)}}{T} \left(\frac{\left[V_{out} + (L_A + \sqrt{L_2 L_A}) \frac{\Delta i_{in(OP)}}{t_{(OP)}} \right] t_{(OP)}}{L_A + L_2 + 2\sqrt{L_2 L_A}} \right) \right]$$

$$i_{in(Avg)} = \frac{V_{out}}{\epsilon V_{in}} \left(\frac{\left[V_{out} + (L_A + \sqrt{L_2 L_A}) \frac{\Delta i_{in(OP)}}{t_{(OP)}} \right] t_{(OP)}^2}{T (L_A + L_2 + 2\sqrt{L_2 L_A})} \right)$$

substituting (2.32)

$$i_{in(Avg)} = \frac{V_{out}}{\epsilon V_{in}} \left(\frac{\left[V_{out} + (L_A + \sqrt{L_2 L_A}) \frac{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{t_{(OP)}}{L_{in}}}{t_{(OP)}} \right] t_{(OP)}^2}{T (L_A + L_2 + 2\sqrt{L_2 L_A})} \right)$$

$$i_{in(Avg)} = \frac{V_{out}}{\epsilon V_{in}} \left(\frac{V_{out} + (L_A + \sqrt{L_2 L_A}) \left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}}}{T (L_A + L_2 + 2\sqrt{L_2 L_A})} t_{(OP)}^2 \right) \quad (2.46)$$

Input Power

The power input as a function of switching period T and duty cycle D can be defined by

$$P_{in} = V_{in} \times i_{in(Avg)}$$

substituting (2.46) and (2.36)

$$P_{in} \approx \frac{V_{out}}{\epsilon} \left[\frac{V_{out} + (L_A + \sqrt{L_2 L_A}) \left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}}}{(L_A + L_2 + 2\sqrt{L_2 L_A}) T} \right] \left[T \frac{\frac{V_{in}}{2(L_{in}+L_A)} \left(D \frac{L_A}{L_{in}} + 1 \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in}+L_A}} \right]^2$$

$$P_{in} \approx \frac{T^2}{T} \frac{V_{out}}{\epsilon} \left[\frac{V_{out} + (L_A + \sqrt{L_2 L_A}) \left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}}}{L_A + L_2 + 2\sqrt{L_2 L_A}} \right] \left[\frac{\frac{V_{in}}{2(L_{in}+L_A)} \left(D \frac{L_A}{L_{in}} + 1 \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in}+L_A}} \right]^2$$

$$P_{in} \approx T \frac{V_{out}}{\epsilon} \left[\frac{V_{out} + (L_A + \sqrt{L_2 L_A}) \left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}}}{L_A + L_2 + 2\sqrt{L_2 L_A}} \right]$$

$$\times \left[\frac{\frac{V_{in}}{2(L_{in}+L_A)} \left(D \frac{L_A}{L_{in}} + 1 \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in}+L_A}} \right]^2 \quad (2.47)$$

where ϵ is the overall efficiency, assumed to be unity for this model.

Output Diode Voltage

The output diodes are subjected to lower current but larger voltages. The voltage across the conducting diode will simply be V_F however the anode of the non-conducting diode is pulled negative by the open coil and so has a peak reverse voltage of

$$V_{D_{rr}} = V_{out} + V_B$$

as shown in Figure 2.13.

During $t_{(OP)}$ the voltage on the anode of the non-conducting diode V_{anode} is pulled negative by the open coil by an amount V_B where

$$V_B = \eta \frac{V_{out}}{2 + \eta}$$

thus

$$V_{D_{rr}} = V_{out} \left(1 + \frac{\eta}{2 + \eta} \right) \quad (2.48)$$

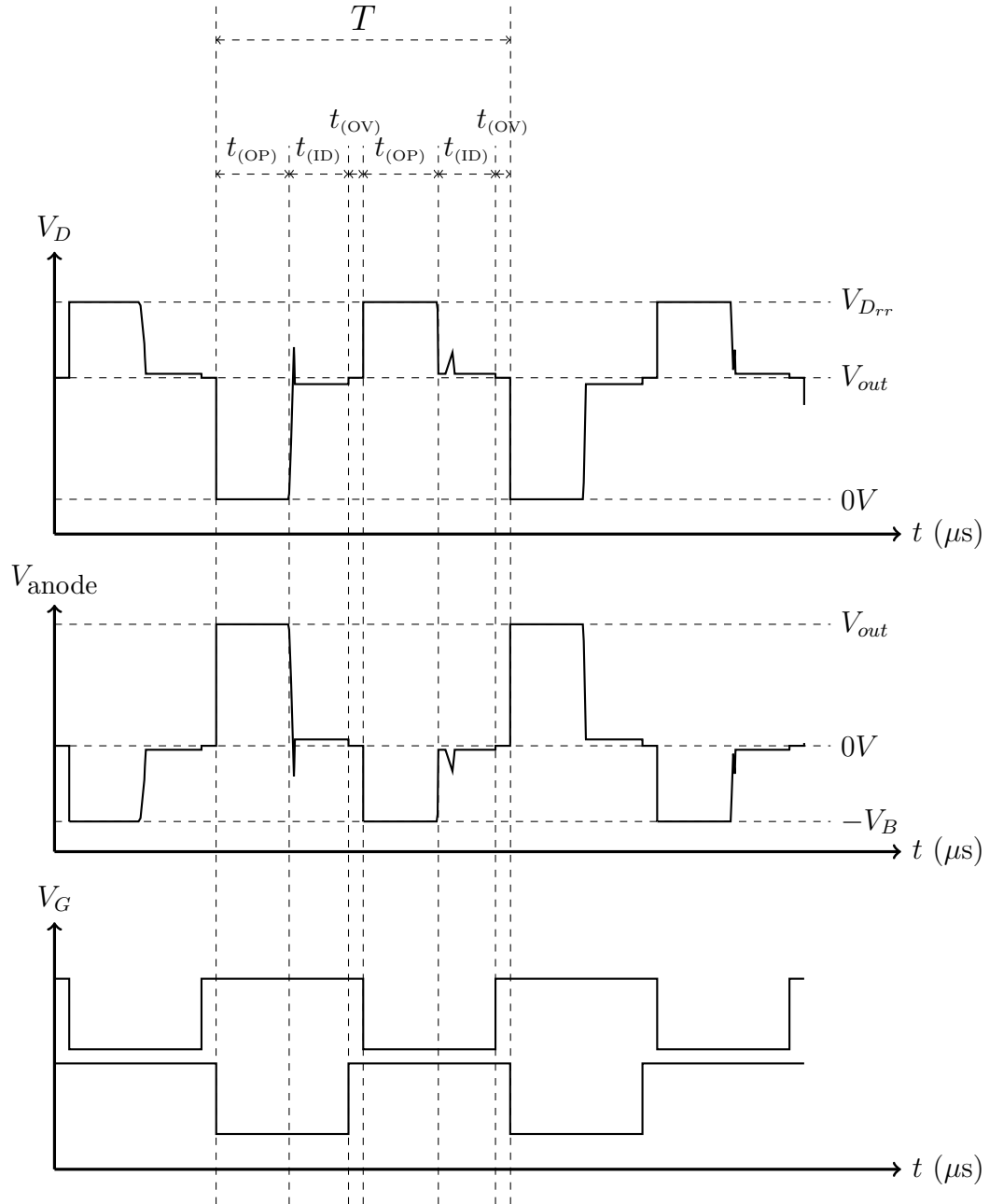


Fig. 2.13: Output diode voltage waveforms over a switching period

All values of the input current over time $\frac{T}{2}$ as shown in Figure 2.6 can now be quantified using the following equation set

$$t_{(\text{OP})} = T \frac{\frac{V_{in}}{2(L_{in}+L_A)} \left(D \frac{L_A}{L_{in}} + 1 \right)}{\left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} + \frac{V_{in}}{L_{in}+L_A}} \quad (2.49)$$

$$\Delta i_{in(\text{OP})} = i_{in(\text{max})} - i_{in(\text{min})} = \left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{t_{(\text{OP})}}{L_{in}} \quad (2.50)$$

$$L_2 = L_A + L_B + 2\sqrt{L_A L_B} \quad (2.51)$$

$$i_{in(\text{Avg})} = \frac{V_{out}}{\epsilon V_{in}} \left(\frac{V_{out} + (L_A + \sqrt{L_2 L_A}) \left(\frac{V_{out}}{2+\eta} - V_{in} \right) \frac{1}{L_{in}} t_{(\text{OP})}^2}{T (L_A + L_2 + 2\sqrt{L_2 L_A})} \right) \quad (2.52)$$

$$i_{in(\text{max})} = i_{in(\text{Avg})} + \frac{\Delta i_{in(\text{OP})}}{2} \quad (2.53)$$

$$i_{in(\text{min})} = i_{in(\text{Avg})} - \frac{\Delta i_{in(\text{OP})}}{2} \quad (2.54)$$

$$\Delta i_{in(\text{OV})} = i_{in(\text{max})} - i_{in\alpha} = \frac{V_{in}}{L_{in}} D \frac{T}{2} \quad (2.55)$$

$$\Delta i_{in(\text{ID})} = i_{in\alpha} - i_{in(\text{min})} = \frac{V_{in}}{L_{in} + L_A} \left[\frac{T}{2} (1 - D) - t_{(\text{OP})} \right] \quad (2.56)$$

$$i_{in\alpha} = i_{in(\text{min})} + \Delta i_{in(\text{ID})} = i_{in(\text{max})} - \Delta i_{in(\text{OV})} \quad (2.57)$$

All values of current through coils L_{A1}, L_{A2} over time $\frac{T}{2}$ as shown in Figure 2.8 can now be quantified using the following equation set

$$i_{out(max)} = \Delta i_{out} = \frac{\left[V_{out} + (L_A + \sqrt{L_2 L_A}) \frac{\Delta i_{in(OP)}}{t_{(OP)}} \right] t_{(OP)}}{L_A + L_2 + 2\sqrt{L_2 L_A}} \quad (2.58)$$

$$i_{A(max)} = i_{in(max)} \quad (2.59)$$

$$i_{A\alpha} = i_{in\alpha} \quad (2.60)$$

$$i_{A\beta} = i_{in(min)} \quad (2.61)$$

$$i_{A\gamma} = i_{in(max)} - i_{out(max)} \quad (2.62)$$

The node voltage V_{N_x} and switch voltages V_{S_x} over time $\frac{T}{2}$ can be determined using the following equation set

$$V_{N(OV)} = 0 \quad (2.63)$$

$$V_{N(OP)} = \frac{V_{out}}{2 + \eta} \quad (2.64)$$

$$V_{N(ID)} = L_A \frac{\Delta i_{in(ID)}}{\frac{T}{2}(1 - D) - t_{(OP)}} \quad (2.65)$$

The switch voltages are always given by

$$V_{S_x} = 2V_{N_x} \quad (2.66)$$

and peak blocking voltage required by the diodes is given by

$$V_{D_{rr}} = V_{out} \left(1 + \frac{\eta}{2 + \eta} \right) \quad (2.67)$$

A mathematical model of the proposed topology under ideal conditions has been developed in this section. Equations have been derived for the relevant voltages and currents in the circuit and are validated against simulation data in Appendix .7 and .6. In order to test the validity of these claims in the real world, a prototype has been constructed and tested.

3. PROTOTYPE EXPERIMENTATION

A mathematical model of the proposed topology under ideal conditions has been developed in Section 2. Equations have been derived for the relevant voltages and currents and are validated against simulation data in Appendix .7 and .6. In order to test the validity of these claims in the real world, this section covers the construction and testing of a prototype.

High levels of loss were expected during primary testing and so over-rated components were used. Specifically, MOSFETs and diodes with breakdown voltages much higher than the input or output voltages were used to ensure survival in the presence of high voltage spikes. Higher breakdown voltage MOSFETs have higher ON-resistance which leads to greater loss when conducting large currents. Test involving input currents up to 10A were performed and caused significant heating of the MOSFETs which were bolted to the metal chassis to dissipate this excess heat. At this early stage poor efficiency was expected but component survival was prioritised.

A DC bench-top power supply was used to provide a stable input voltage. An electronic load was used which varies its resistance to keep the output voltage V_{out} at a constant set point.

Rohde & Schwarz HM8115-2 programmable power meters were used to measure the average input and output power. The HM8115-2 has a claimed accuracy to within $\pm 0.4\%$ for voltage and current readings, and $\pm 0.8\%$ for power readings, according to the technical data-sheet provided by the manufacturer. While any appliance will have a certain amount of uncertainty it is discounted here as it is low enough so as to have no significant effect on the experiment or results. Figure 3.1 shows the prototype testing assembly block diagram.

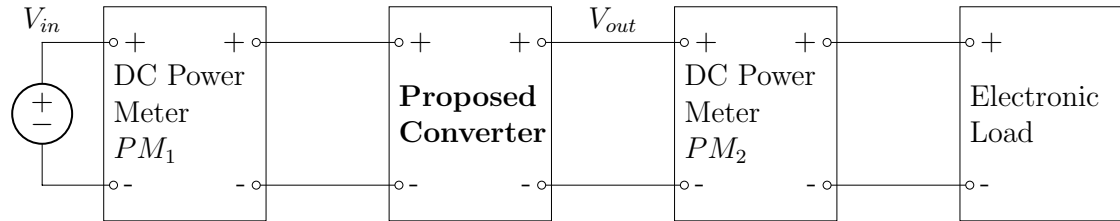


Fig. 3.1: Block diagram of prototype assembly

The magnetic assembly is the basis of the loss analysis presented in Sections 3.0.2, 3.0.3, 3.0.4. Toroidal cores were used in the first prototype, characterised in Appendix .4. The Wayne-Kerr 3245 precision inductance analyser in combination with the Wayne-Kerr 3220 20A bias unit (Figure .8) was used to perform the analysis. The analyser applies a small magnitude alternating current at a programmable frequency combined with a programmable DC bias current up to 20A. The results show that the Sendust MS-157125-2 material used for the toroidal transformer does not saturate at a switching frequency of 100kHz and a DC bias current up to 9A (Figure .10) which was the maximum applied during the experiment. The Sendust MS-106125-2 material used for the input storage inductor did begin to saturate at a switching frequency of 100kHz and a bias current of up to 8A which manifested as a drop in inductance as shown in Figure .9. This did not matter as it can be proven from the derivations in Section 2.0.3 and the results displayed in Appendix .7 that the input inductor value only affects the input current ripple significantly.

An “I-prober 520” non-contact hall-effect current probe from Aim Instruments was used to measure the intermediate currents in the circuit. The I-prober 520 has an accuracy of 3% according to the technical data-sheet. It works by sensing the magnetic field emitted by a current travelling in a conductor and produces a proportional electrical output which can be monitored on an oscilloscope. Because it is sensitive to magnetism makes it subject to offset errors caused by the earth’s magnetic field. To eliminate this problem the probe was held in the air well away from any magnetism sources and the trim was set until the offset was nullified on all three axes.

The resulting waveforms captured using the probe are shown in Figure 3.2.

Being hand-held, getting a decent reading required a number of attempts the best of which are presented in Figure 3.2.

Also because the probe is non-contact there is a less than ideal coupling between the probe and the measured conductor which will also introduce error or up to 5% into the measurement according to the technical data-sheet.

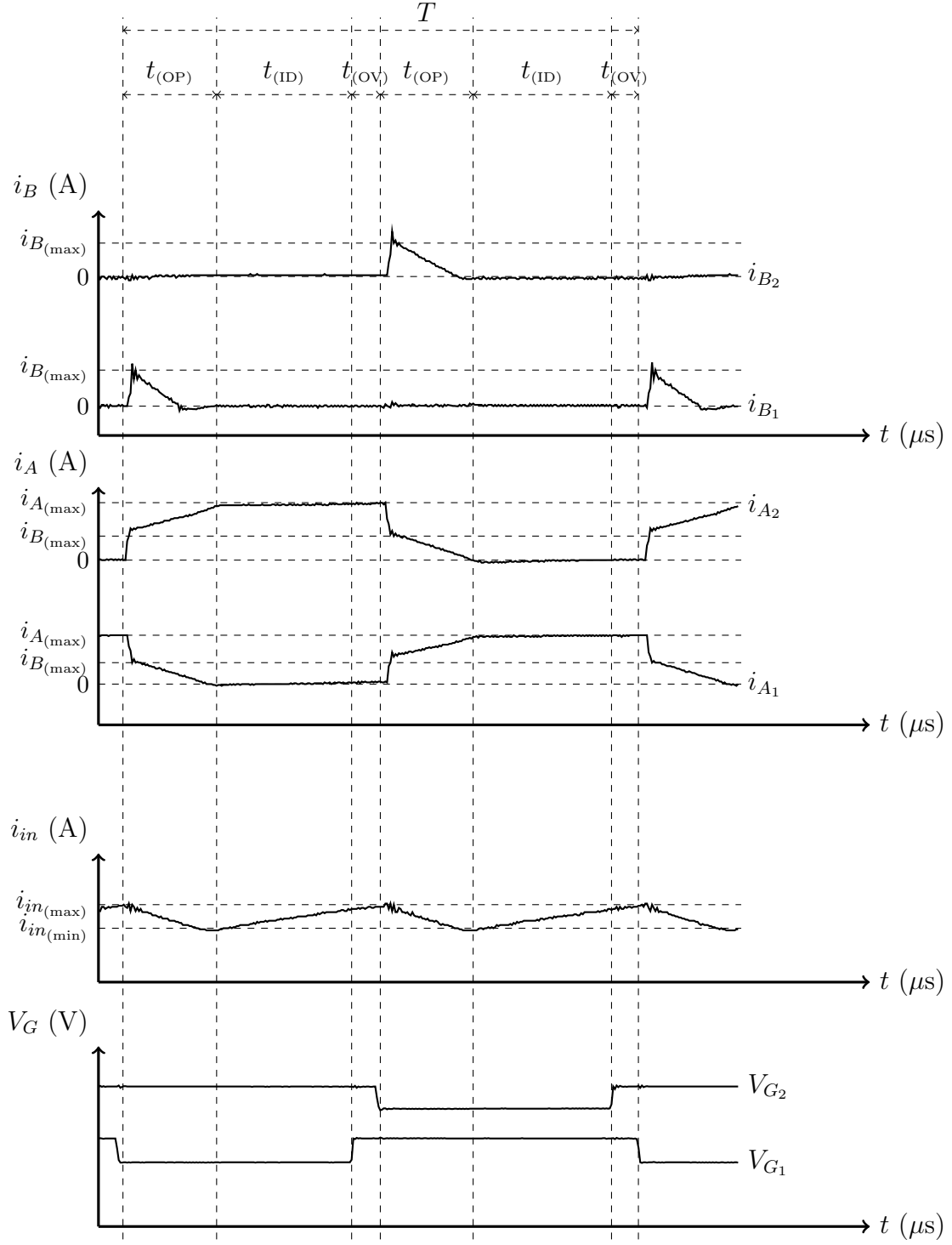


Fig. 3.2: Current waveforms measured from final prototype assembly
 $V_{in} = 28\text{V}$, $V_{out} = 250\text{V}$, $L_{in} = 36\mu\text{H}$, $L_A = 10\mu\text{H}$, $L_B = 130\mu\text{H}$,
 $T = 18\mu\text{s}$, $t_{(OP)} \approx 5\mu\text{s}$

Using eddy current analysis presented by Dowell [98–100] higher AC loss can result from multiple parallel conductors in transformer windings.

This is investigated further in Section 3.0.2 and illustrated in Figure 3.6.

3.0.1 Loss Analysis

The initial prototype was constructed with low quality components and magnetics in order to make loss quantification easier. The more loss there is in the circuit the easier it is to measure. Also the components responsible for the loss become apparent through heating which can be measured using a thermal camera or even just by touching.

The prototype assembly as tested in this section is shown in Figure 3.3 and the

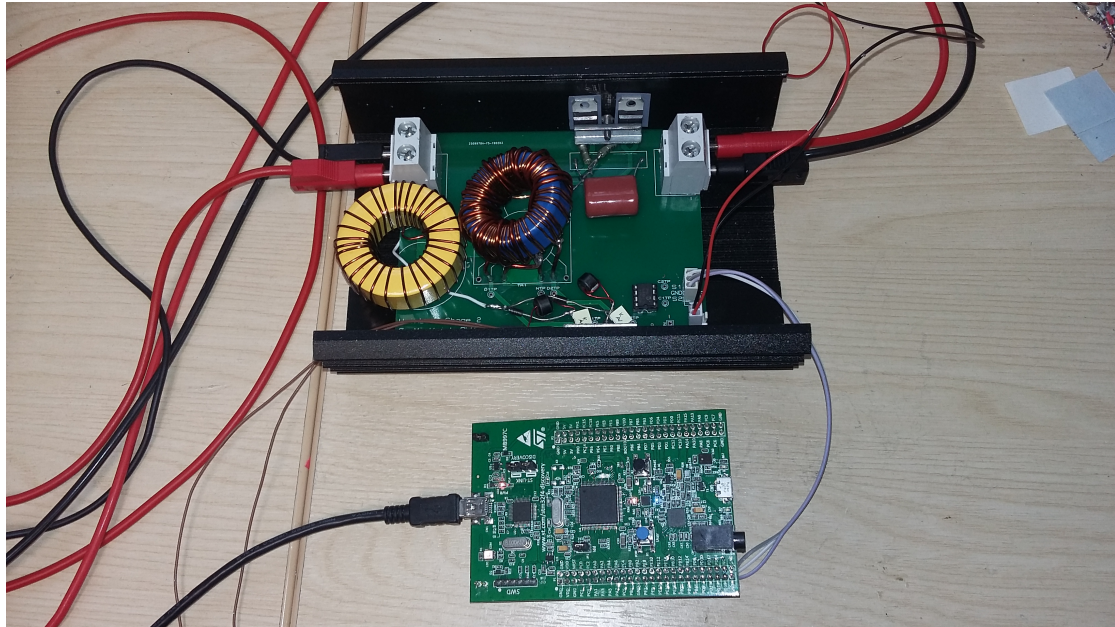


Fig. 3.3: Constant output voltage prototype assembly with microcontroller based switching control

input and output measurements of the prototype under test is shown in Figure 3.4. The output voltage is clamped to 150V in this experiment.

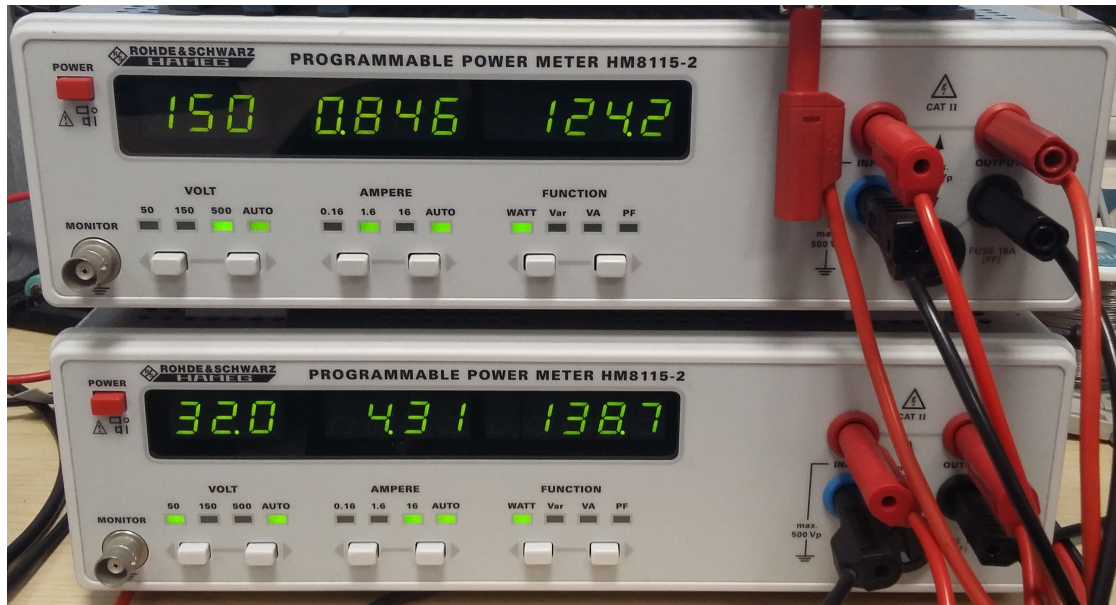


Fig. 3.4: Measured input (bottom) and output (top) power during prototype experimentation

Input Voltage: 32 V
Input Current: 4.31 A
Input Power: 138.7 W

Output Voltage: 150 V
Output Current: 0.846 A
Output Power: 124.2 W

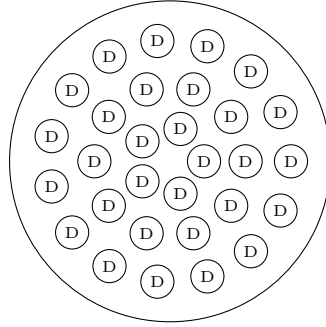
3.0.2 *Electrical Losses in Magnetic Windings*

There are electrical losses associated with the inductive windings. When DC passes through a conductor of Cross-Sectional Area (CSA) a then it can be assumed that the current carriers distribute evenly throughout (Figure 3.5a) and the resistance of a conductor of total length l is given as

$$R_{dc} = \rho \frac{l}{a} \quad (3.1)$$

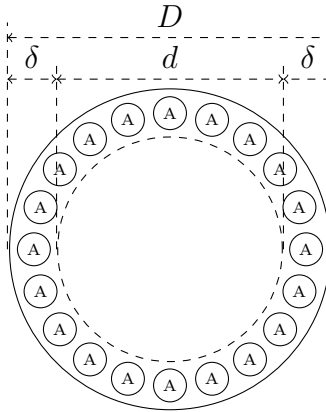
where ρ is the resistivity of the conductor material which is constant assuming the temperature does not fluctuate significantly. When AC passes through the same conductor a phenomenon called the “Skin Effect” [98] causes the current density around the outside of the conductor to become higher than that in the centre (Figure 3.5b). Effectively all the current carriers migrate to the edge of the conductor leaving very few in the centre. This effect becomes more pronounced as the AC frequency increases. The current carriers form a layer around the edge of the conductor of thickness δ which is termed the “Skin Depth”. For AC this reduces the effective CSA of the conductor which increases the resistance as shown in Figure 3.5b .

Also when many conductors are tightly wound together, such as is the case with transformer windings, they become subjected to “Current Crowding” (aka the “Proximity Effect”). This is where the magnetic fields generated by the conductors generate eddy currents in adjacent conductors causing an uneven distribution of current carriers (Figure 3.6) and an increase in AC resistance. Figure 3.6d shows that in some cases the proximity effect can result in conductors carrying no current at all. This effect also increases with frequency.



‘D’ represents DC current carriers

(a) Cross-section of a conductor showing the distribution of constant current carriers



‘A’ represents AC current carriers

$$\delta = \frac{D - d}{2}$$

(b) Cross-section of a conductor showing the distribution of time-varying current carriers

Fig. 3.5: Illustration of the Skin Effect in a single conductor

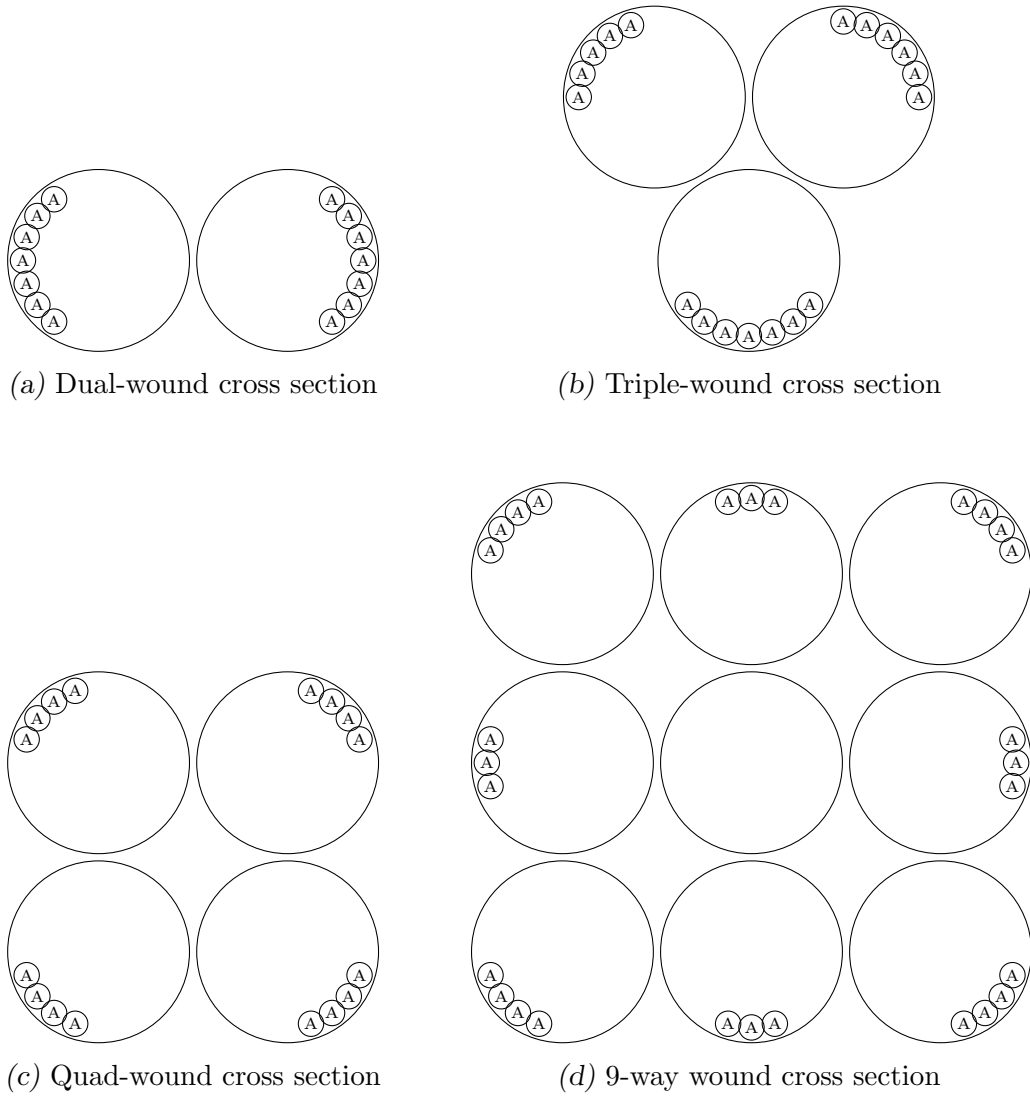


Fig. 3.6: Illustration of the proximity effect on multiple conductor windings
 'A' represents AC current carriers

From the analysis presented in [98–100] the total AC power loss P in a magnetic winding over a range of N_h harmonic frequencies can be given by

$$P = R_{dc} \left(i_{dc}^2 + \sum_{n=1}^{N_h} [i_n^2 R_{acn}] \right) \quad (3.2)$$

where R_{acn} is the AC resistance at the n^{th} harmonic and i_n is the AC current magnitude at the n^{th} harmonic.

In the constructed prototype the following parameters were used

$$\begin{aligned} L_{in} &= 100 \mu\text{H} & (29 \text{ turns}) \\ L_A &= 20 \mu\text{H} & (10 \text{ turns}) \\ L_B &= 80 \mu\text{H} & (20 \text{ turns}) \\ V_{in} &= 32 \text{ V} \\ V_{out} &= 150 \text{ V} \\ T &= 10 \mu\text{s} \\ D &= 0.1 \end{aligned}$$

Any winding is made up of N turns of circular copper conductor of diameter D_c . To aid mathematical modelling a set of N closely wound conductors with a diameter D_c can be modelled as a single conductor or “foil” of width w and thickness d which is derived from the physical diameter as

$$d = \sqrt{\frac{\pi}{4}} D_c$$

Note that the equivalent modelled foil width w is different from the physical width. The ratio of the two widths serves as a scaling factor termed the “Porosity Factor” η_i which is given by

$$\eta_i = \frac{Nd}{w}$$

Due to the skin effect the effective conducting area of the conductor is less than its physical size. If the physical thickness of the conductor is d and the skin depth at the n^{th} harmonic is δ_n then the ratio Δ is given as

$$\Delta = \frac{d}{\delta_n}$$

where

$$\delta_n = \sqrt{\frac{1}{\pi f_n \mu_0 \sigma_w}} \quad (3.3)$$

$$\mu_0 = 4\pi \times 10^{-7}$$

The conductivity of copper $\sigma_{(\text{Cu})}$ is constant, given as

$$\sigma_{(\text{Cu})} = 59.52 \times 10^6 \frac{\text{S}}{\text{m}}$$

and the subsequent resistivity value is

$$\rho_{(\text{Cu})} = 1.68 \times 10^{-8} \Omega\text{m}$$

The porosity factor η_i is a scaling value which relates the physical properties of the conductors and their equivalent properties when modelled as a single foil. The conductivity will also be scaled giving an effective conductivity

$$\sigma_w = \eta_i \sigma_{(\text{Cu})}$$

The prototype has a combination of single layer wound ($p = 1$) and dual-layer wound ($p = 2$) coils and alternates between the two states multiple times within a single switching period. Higher loss is incurred when $p = 2$ therefore as a “worst case” scenario it is assumed that $p = 2$ always.

The AC resistance R_{ac_n} at the n^{th} harmonic frequency is defined in [99] as

$$R_{ac_n} = \sqrt{n}\Delta \left[\frac{\sinh(2\sqrt{n}\Delta) + \sin(2\sqrt{n}\Delta)}{\cosh(2\sqrt{n}\Delta) - \cos(2\sqrt{n}\Delta)} + \frac{2(p^2 - 1)}{3} \cdot \frac{\sinh(\sqrt{n}\Delta) - \sin(\sqrt{n}\Delta)}{\cosh(\sqrt{n}\Delta) + \cos(\sqrt{n}\Delta)} \right] \quad (3.4)$$

Fourier analysis of current waveforms for all significant windings is provided in Appendix .5 and a dataset of harmonic magnitude values are provided in Table .1.

Outer diameter OD_{IND}	47mm
Inner diameter ID_{IND}	23mm
Height h_{IND}	18mm
Electrical length of winding l_{IND} (m)	$\left(\frac{OD_{\text{IND}} - ID_{\text{IND}} + 2h_{\text{IND}}}{1000} \right) N = 0.060N$
Magnetic path length $l_{m\text{IND}}$ (m)	0.11
Magnetic core volume $V_{m\text{IND}}$ (cm ³)	$\frac{\pi}{4000} (OD_{\text{IND}} - ID_{\text{IND}})^2 h_{\text{IND}} = 8.143$
$\mu_{r\text{IND}}$	75

Tab. 3.1: Properties of the MicroMetals T184-26 iron powder core as supplied in the MicroMetals T184-26 datasheet.

N is the number of turns.

If 1mm diameter ($D_c = 0.001$ m) single core enamelled copper wire is used to create the windings then its CSA is given as

$$a = \frac{\pi D_c^2}{4} = 785 \times 10^{-9} \text{ m}^2 \quad (3.5)$$

Outer diameter OD_{TR}	40mm
Inner diameter ID_{TR}	23mm
Height h_{TR}	15mm
Electrical length of winding l_{TR} (m)	$\left(\frac{OD_{\text{TR}} - ID_{\text{TR}} + 2h_{\text{TR}}}{1000}\right) N = 0.048N$
Magnetic path length $l_{m\text{TR}}$ (m)	0.10
Magnetic core volume $V_{m\text{TR}}$ (cm ³)	$\frac{\pi}{4000} (OD_{\text{TR}} - ID_{\text{TR}})^2 h_{\text{TR}} = 3.655$
$\mu_{r\text{TR}}$	125

Tab. 3.2: Properties of the MS-157125-2 Sendust powder core as supplied in the “Chang Sung Corporation catalogue.”
 N is the number of turns.

If the number of turns used for each winding is

$$\begin{aligned} N_{(L_{in})} &= 29 \\ N_{(L_A)} &= 10 \\ N_{(L_B)} &= 20 \end{aligned}$$

then using the physical properties of the magnetic cores supplied in Tables 3.1 and 3.2, the length of the winding l is given by

$$\begin{aligned} l_{(L_{in})} &= l_{\text{IND}} N_{(L_{in})} = 1.740 \text{ m} \\ l_{(L_A)} &= l_{\text{TR}} N_{(L_A)} = 0.481 \text{ m} \\ l_{(L_B)} &= l_{\text{TR}} N_{(L_B)} = 0.963 \text{ m} \end{aligned}$$

The DC resistance R_{dc} is given by (3.1) and (3.5) as

$$\begin{aligned} R_{dc(L_{in})} &= \rho_{(\text{Cu})} \frac{l_{(L_{in})}}{a} = 0.037 \text{ } \Omega \\ R_{dc(L_A)} &= \rho_{(\text{Cu})} \frac{l_{(L_A)}}{a} = 0.010 \text{ } \Omega \\ R_{dc(L_B)} &= \rho_{(\text{Cu})} \frac{l_{(L_B)}}{a} = 0.021 \text{ } \Omega \end{aligned}$$

A dataset of AC resistance values is generated over N_h harmonic frequencies using (3.4), shown in Table 3.3.

Frequency (kHz)	R_{ac_n} (Ω)
100	12.00
200	23.04
300	34.58
400	46.11
500	57.64
600	69.17
700	80.69
800	92.22
900	103.75
1000	115.28
1100	126.80
1200	138.33
1300	149.86
1400	161.39
1500	172.91
1600	184.44
1700	195.97
1800	207.50
1900	219.02
2000	230.55
2100	242.08
2200	253.61
2300	265.13
2400	276.66
2500	288.19
2600	299.72
2700	311.24
2800	322.77
2900	334.30
3000	345.83

Tab. 3.3: AC resistance values over N_h harmonics

Figure 3.6 assumes the field is uniform across the conductor. When a ferromagnetic material is brought into very close proximity the current concentrates around the contacting surface of the conductor. When the conductor is wound around a core this causes the current to concentrate around the inside edge of the coil. The effects of the ferromagnetic material on eddy current losses in toroidal wound inductors is investigated in the MicroMetals App-note [101].

An inductor has physical parameters, conductor diameter D_c , number of turns N , magnetic path length l_m and relative permeability μ_r . The fundamental switching frequency f_0 determines the skin depth at that frequency δ_0 , given by (3.3), and is a major factor in the AC resistance R_{ac} .

Determining the AC resistance R_{ac} is covered in [99] however the investigations carried out in [101] brings to attention how the physical layout of the conductors around the ferromagnetic material affects the interaction of the magnetic flux lines which consequently affects the eddy current losses incurred by the material. These eddy current losses introduce a margin of error into the AC resistance values calculated using (3.4). They are dependant on factors which it is very difficult to measure on a physical assembly such as conductor pitch p and conductor proximity to the core s .

For a toroid the conductor pitch p can be approximated from the number of turns N and the magnetic path length l_m as

$$p = \frac{l_m}{N}$$

Ideally the proximity of the conductor to the ferromagnetic material s would be zero. Assuming the conductor is wound tightly around the core the proximity of the conductor to the ferromagnetic material s is limited by the enamel coatings on both the conductor $s_{(\text{cond})}$ and the core $s_{(\text{core})}$

$$s = s_{(\text{cond})} + s_{(\text{core})}$$

The thickness of the conductor and core enamel coatings are supplied in the respective data-sheets.

It was found by [101] that the eddy current contribution to the AC resistance is dependant on three main ratios of physical parameters. The ratio of core proximity s to conductor diameter D_c $\left(\frac{s}{D_c}\right)$, conductor pitch p to conductor diameter D_c $\left(\frac{p}{D_c}\right)$ and conductor diameter D_c to skin depth at the fundamental frequency δ_0 $\left(\frac{D_c}{\delta_0}\right)$.

The error which these parameters introduce into the AC resistance calculation is quantified in [101] as two variables, $K1$ which quantifies the upper bound error

	L_{in}	L_A	L_B
μ_r	75	125	125
N	29	10	20
D_c (mm)	1	1	1
$s_{(cond)}$ (mm)	0.04	0.04	0.04
$s_{(core)}$ (mm)	0.315	0.405	0.405
s (mm)	0.355	0.445	0.445
f_0 (kHz)	200	100	100
δ_0 (mm)	0.145	0.205	0.205
l_m (mm)	110	100	100
p (mm)	3	10	5
$\frac{s}{D_c}$	0.335	0.445	0.445
$\frac{p}{D_c}$	3	10	5
$\frac{D_c}{\delta_0}$	7	5	5
$K1$	1.03	1.9	1.17
$K2$	0.81	0.65	0.78

Tab. 3.4: Parameters involved in eddy current loss analysis from [101]

and $K2$ which quantifies the lower bound error. These parameters as they apply to the circuit windings L_{in} , L_A , and L_B are shown in Table 3.4.

$K1$ and $K2$ are only calculated for the fundamental frequency in Table 3.4 but can be repeated for all harmonic frequencies to determine the uncertainty introduced by eddy currents. This means the calculated AC resistance values in Table 3.3 could be anything up to $K1$ times larger or $K2$ times smaller in reality.

If the DC component of the currents in the windings is

$$\begin{aligned} i_{dc(L_{in})} &= 4.040 \text{ A} \\ i_{dc(L_A)} &= 2.020 \text{ A} \\ i_{dc(L_B)} &= 0.429 \text{ A} \end{aligned}$$

then from (3.2) the combined AC and DC losses in each winding is

$$\begin{aligned} P_{(L_{in})} &= 0.607421 \text{ W} \\ P_{(L_A)} &= 0.042010 \text{ W} \\ P_{(L_B)} &= 0.003783 \text{ W} \end{aligned}$$

The overall power loss in the circuit contributed by the windings is

$$P_{elec(Avg)} = P_{(L_{in})} + P_{(L_A)} + P_{(L_B)} = 0.653214 \text{ W} \quad (3.6)$$

3.0.3 Magnetic Losses

When AC current is passed through a magnetising coil it induces a magnetic flux in the core material. As the current changes direction so does the flux. Each time the flux changes direction a loss is incurred as the magnetic domains inside the ferrous material becomes re-polarised.

In the proposed topology the input current has a DC bias and never goes negative during steady-state operation. This means the flux in the inductor core increases and decreases in magnitude but never reverses direction so the associated magnetic losses are reduced.

When a current i flows through an inductive winding a coercive force H is produced which subsequently produces a magnetic flux of density B . The coercive force H as a function of current i is given as

$$H \left(\frac{\text{A}}{\text{m}} \right) = N \frac{i}{l_m} \quad (3.7)$$

where N is the number of turns that make up the inductive coil and l_m is the magnetic path length of the core in question; usually specified in the technical data-sheet supplied by the core manufacturer. The magnetic flux density B as a function of coercive force H is given as

$$B \text{ (T)} = \mu_0 \mu_r H \quad (3.8)$$

where μ_0 is the permeability of free space

$$\mu_0 = 4\pi \times 10^{-7}$$

and μ_r is the relative permeability of the magnetic core material.

The flux in the core will be the resultant of all the coercive forces from all the active coils. If the number of turns used for each winding in the constructed prototype is

$$\begin{aligned} N_{(L_{in})} &= 29 \\ N_{(L_A)} &= 10 \\ N_{(L_B)} &= 20 \end{aligned}$$

the resultant coercive force will be given from (3.7) as

$$\begin{aligned} H_{IND} \left(\frac{\text{A}}{\text{m}} \right) &= N_{(L_{in})} \frac{i_{(L_{in})}}{l_{m_{IND}}} \\ H_{TR} \left(\frac{\text{A}}{\text{m}} \right) &= \frac{1}{l_{m_{TR}}} \left[\left(i_{(L_{A1})} + i_{(L_{A2})} \right) N_{(L_A)} + \left(i_{(L_{B1})} + i_{(L_{B2})} \right) N_{(L_B)} \right] \end{aligned}$$

and plotted in Figures 3.7, 3.8 which shows how it oscillates between a maxima H_{\max} to a minima H_{\min} when operating in steady state.

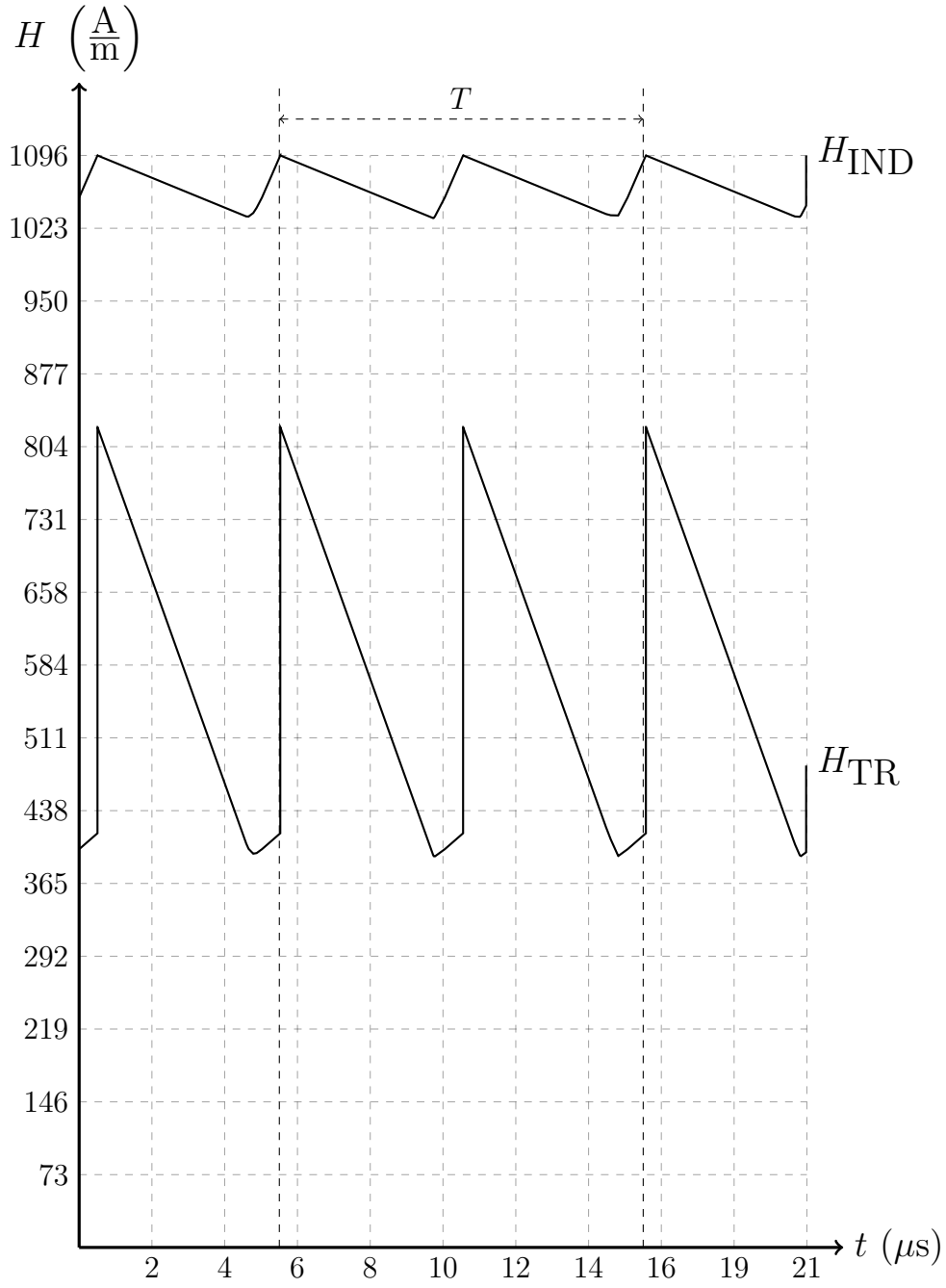


Fig. 3.7: Plot of magnetic field strength in the magnetic cores over time using simulation data

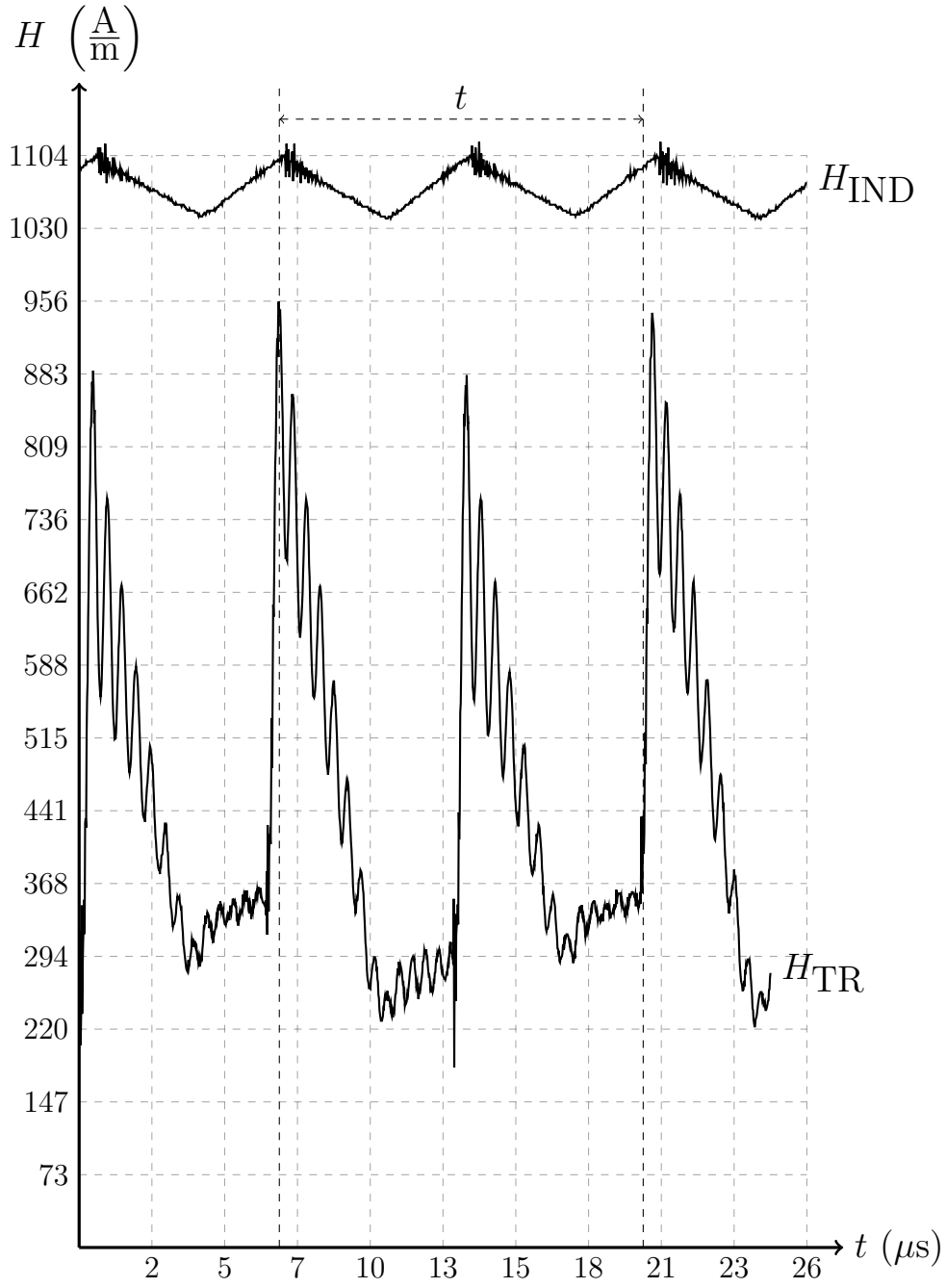


Fig. 3.8: Plot of magnetic field strength in the magnetic cores over time using real data

$$H_{\text{IND}_{\text{max}}} = 1104 \left(\frac{\text{A}}{\text{m}} \right)$$

$$H_{\text{IND}_{\text{min}}} = 1040 \left(\frac{\text{A}}{\text{m}} \right)$$

$$H_{\text{TR}_{\text{max}}} = 930 \left(\frac{\text{A}}{\text{m}} \right)$$

$$H_{\text{TR}_{\text{min}}} = 241 \left(\frac{\text{A}}{\text{m}} \right)$$

This can then be converted into a plot of magnetic flux density using (3.8) plotted in Figures 3.9, 3.10 which oscillates between a maxima B_{max} and minima B_{min}

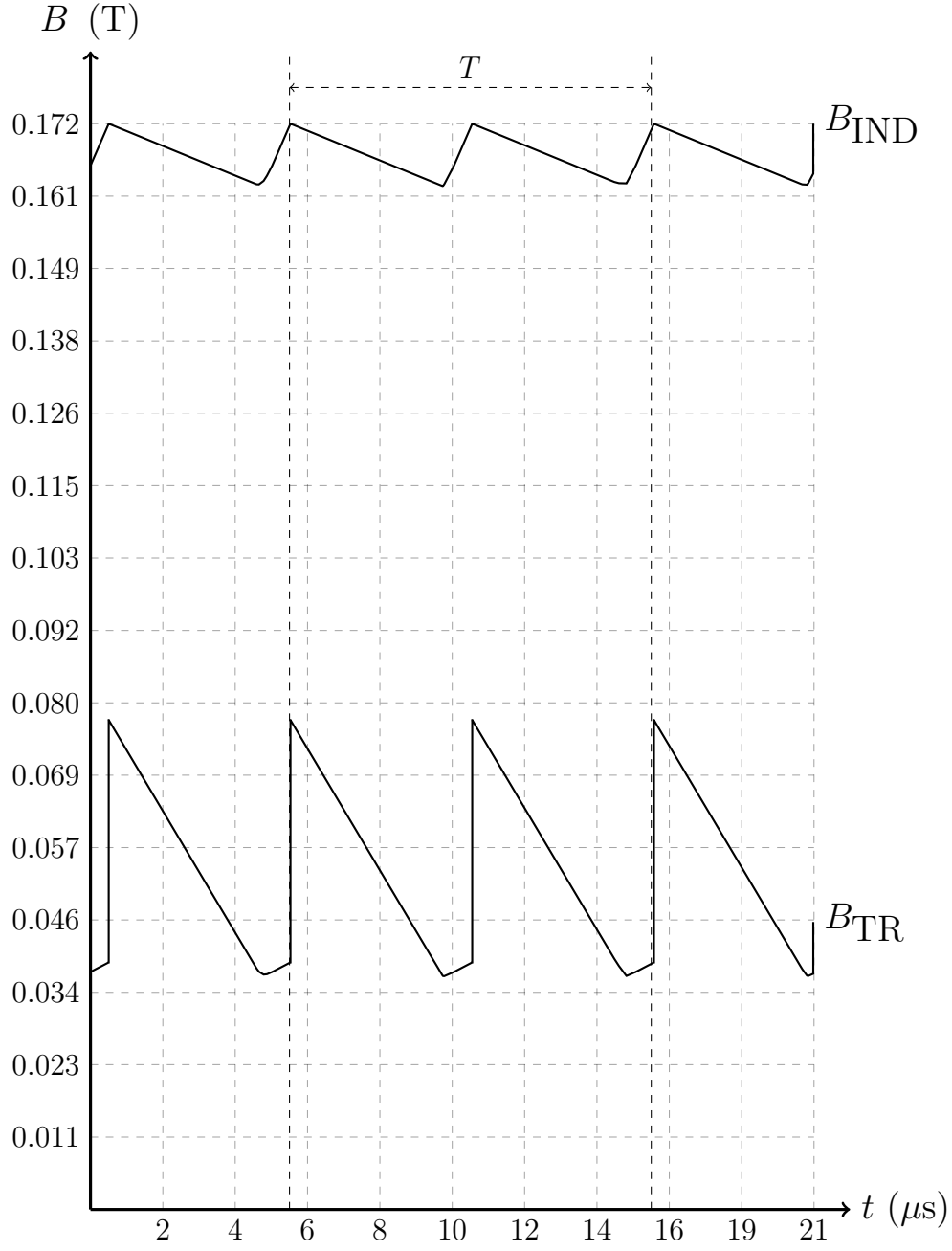


Fig. 3.9: Plot of flux density in the magnetic cores over time using simulation data

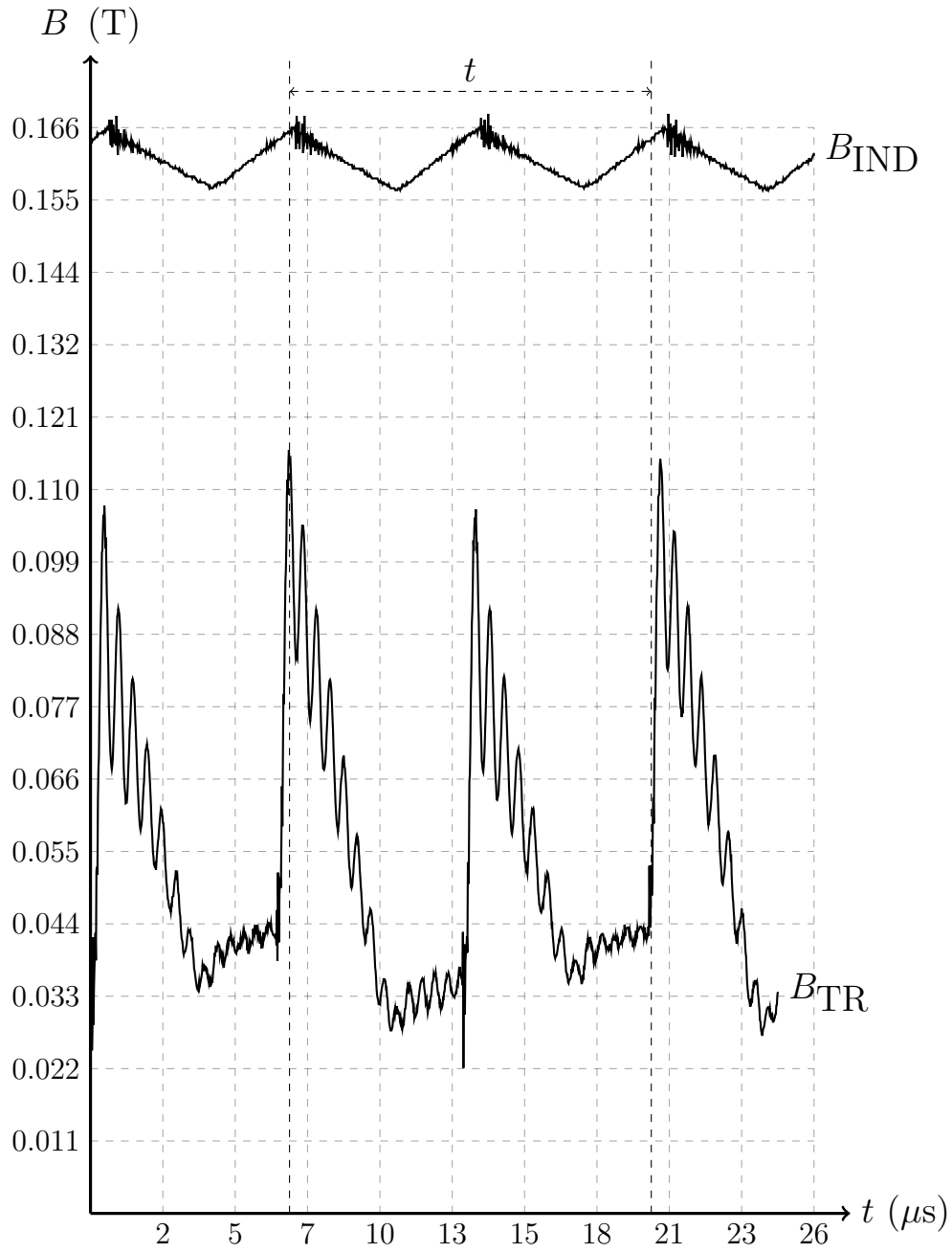


Fig. 3.10: Plot of flux density in the magnetic cores over time using real data

$$\begin{aligned}
B_{\text{IND}_{\text{max}}} &= 0.1656 \text{ (T)} = 1656 \text{ (G}_S\text{)} \\
B_{\text{IND}_{\text{min}}} &= 0.1561 \text{ (T)} = 1560 \text{ (G}_S\text{)} \\
B_{\text{TR}_{\text{max}}} &= 0.1133 \text{ (T)} = 1132 \text{ (G}_S\text{)} \\
B_{\text{TR}_{\text{min}}} &= 0.0294 \text{ (T)} = 293 \text{ (G}_S\text{)}
\end{aligned}$$

This can be converted to a power-loss-per-unit-volume figure using the conversion chart in Figures 3.11 and 3.12

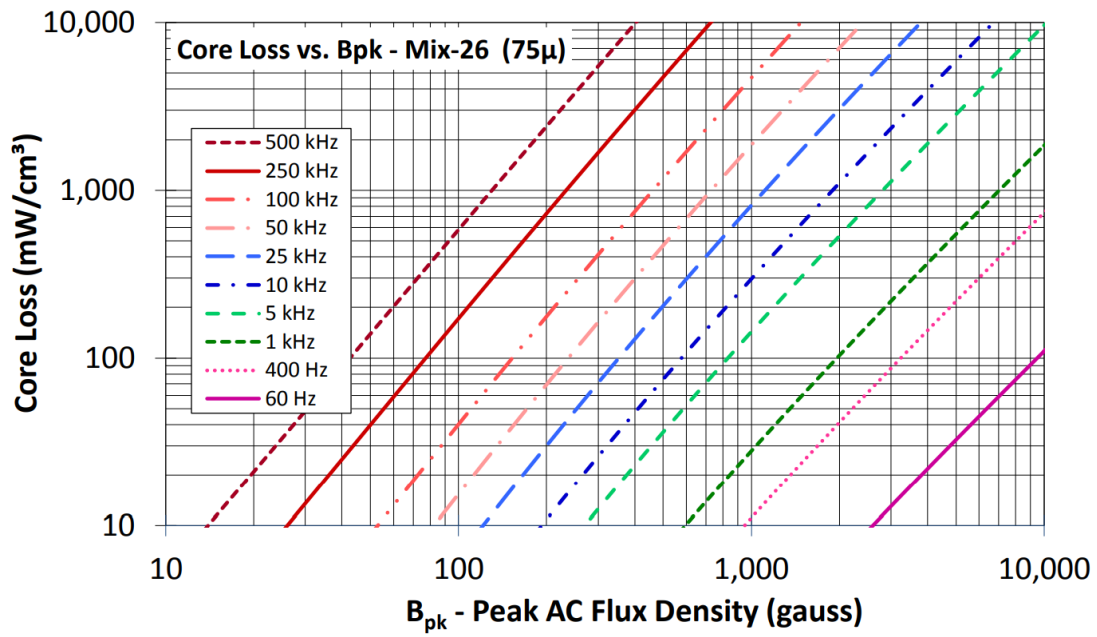


Fig. 3.11: Magnetic flux density to power loss conversion chart for Sendust powder cores provided by the MicroMetals T184-26 datasheet.

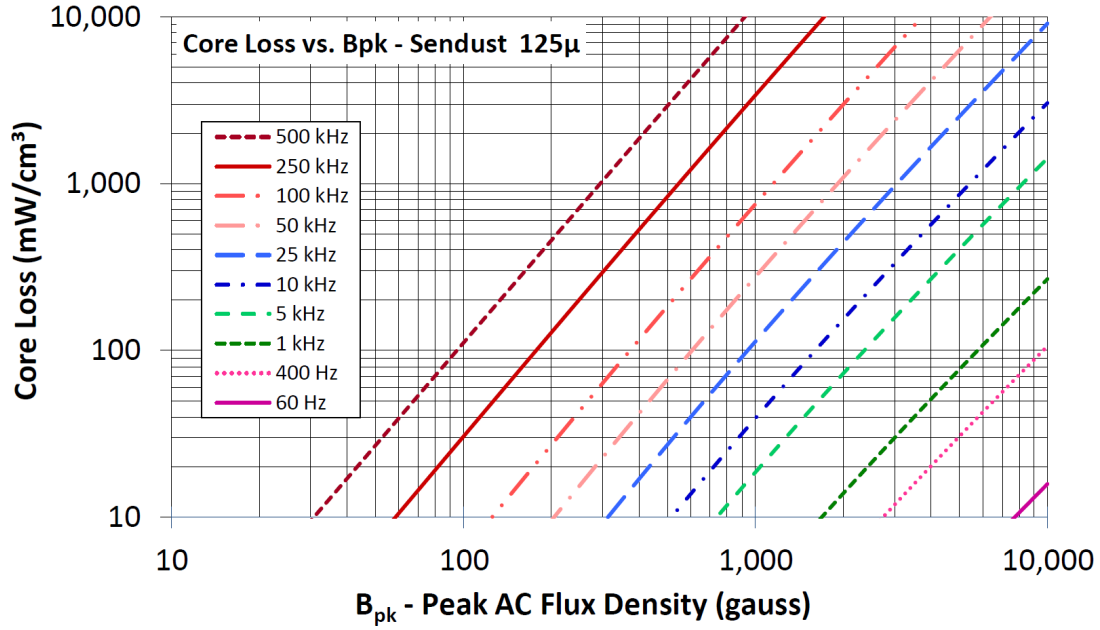


Fig. 3.12: Magnetic flux density to power loss conversion chart for Sendust powder cores provided by MicroMetals MS-157125-2 datasheet.

If the switching frequency is 100kHz the fundamental frequency in the transformer core will be 100kHz. The fundamental frequency in the storage inductor core is twice the switching frequency; so 200kHz. From analysis of Figure 3.11 and 3.12 the equations which approximate the conversion from flux density to power loss per-unit-volume for the T184-26 and MS-157125-2 respectively are

$$P_{\text{IND}} \left(\frac{\text{mW}}{\text{cm}^3} \right) = 2.25 B_{\text{IND}} (\text{G}_S) - 350$$

$$P_{\text{TR}} \left(\frac{\text{mW}}{\text{cm}^3} \right) = 1.1 B_{\text{TR}} (\text{G}_S) - 400$$

and from these the loss-per-unit-volume can be determined as

$$\begin{aligned}
 P_{\text{IND}_{\text{max}}} &= 3376 \left(\frac{\text{mW}}{\text{cm}^3} \right) = 3.376 \left(\frac{\text{W}}{\text{cm}^3} \right) \\
 P_{\text{IND}_{\text{min}}} &= 3161 \left(\frac{\text{mW}}{\text{cm}^3} \right) = 3.161 \left(\frac{\text{W}}{\text{cm}^3} \right) \\
 P_{\text{TR}_{\text{max}}} &= 846 \left(\frac{\text{mW}}{\text{cm}^3} \right) = 0.846 \left(\frac{\text{W}}{\text{cm}^3} \right) \\
 P_{\text{TR}_{\text{min}}} &= 76 \left(\frac{\text{mW}}{\text{cm}^3} \right) = 0.077 \left(\frac{\text{W}}{\text{cm}^3} \right)
 \end{aligned}$$

Finally this gives an absolute maximum and minimum power loss for each core of

$$\begin{aligned}
 P_{\text{absIND}_{\text{max}}} &= P_{\text{IND}_{\text{max}}} \times V_{m\text{IND}} = 5.88 \text{ W} \\
 P_{\text{absIND}_{\text{min}}} &= P_{\text{IND}_{\text{min}}} \times V_{m\text{IND}} = 5.51 \text{ W} \\
 P_{\text{absTR}_{\text{max}}} &= P_{\text{TR}_{\text{max}}} \times V_{m\text{TR}} = 3.09 \text{ W} \\
 P_{\text{absTR}_{\text{min}}} &= P_{\text{TR}_{\text{min}}} \times V_{m\text{TR}} = 0.28 \text{ W}
 \end{aligned}$$

an average power loss for each core of

$$\begin{aligned}
 P_{\text{AvgIND}} &= \frac{P_{\text{absIND}_{\text{max}}} + P_{\text{absIND}_{\text{min}}}}{2} = 5.69 \text{ W} \\
 P_{\text{AvgTR}} &= \frac{P_{\text{absTR}_{\text{max}}} + P_{\text{absTR}_{\text{min}}}}{2} = 1.69 \text{ W}
 \end{aligned}$$

and a total magnetic loss of

$$P_{\text{mag(Avg)}} = P_{\text{AvgIND}} + P_{\text{AvgTR}} = 7.38 \text{ W} \quad (3.9)$$

3.0.4 Conduction Losses

The MOSFETs used in the prototype have a stated Drain-to-Source resistance or ‘ON-resistance’ of

$$R_{\text{DSon}} = 0.48\Omega$$

at an operating temperature of 25°C, which is typical ‘room temperature’. This loss analysis was conducted at relatively low power and so the measured temperature of the MOSFETs did not rise above about 35°C, thus the stated value was assumed.

From Figure 3.4 the average input current $i_{in_{Avg}}$ and average output current $i_{out_{Avg}}$ are measured respectively as

$$\begin{aligned} i_{in_{Avg}} &= 4.31 \text{ A} \\ i_{out_{Avg}} &= 0.846 \text{ A} \end{aligned}$$

the average MOSFET drain currents can be quantified as

$$i_{DS1_{Avg}} = i_{DS2_{Avg}} = \frac{i_{in_{Avg}} - i_{out_{Avg}}}{2} \approx 1.732 \text{ A}$$

which will generate an average loss given by

$$\begin{aligned} P_{S1_{Avg}} &\approx \left(i_{DS1_{Avg}}\right)^2 R_{DSon} \\ P_{S2_{Avg}} &\approx \left(i_{DS2_{Avg}}\right)^2 R_{DSon} \end{aligned}$$

$$P_{S(Avg)} = P_{S1_{Avg}} = P_{S2_{Avg}} \approx 1.44 \text{ W} \quad (3.10)$$

At forward currents of <1A, it can be assumed the diode forward voltage V_F approximates to 1V

$$V_F \approx 1 \text{ V}$$

the power dissipation is then given as

$$P_{D(Avg)} = P_{D1_{Avg}} = P_{D2_{Avg}} = \frac{i_{out_{Avg}}}{2} V_F \approx 0.423 \text{ W} \quad (3.11)$$

3.0.5 Switching Losses

When MOSFETs switch on and off, they transition through a semi-conductive state which causes a spike in dissipated power. The power dissipation waveforms through this semi-conductive state are plotted as P_{DSF} and P_{DSR} in Figures 3.13 and 3.14 respectively.

There can be power dissipation before and after the transition occurs but this is classed as steady-state conduction loss which is quantified in Section 3.0.4.

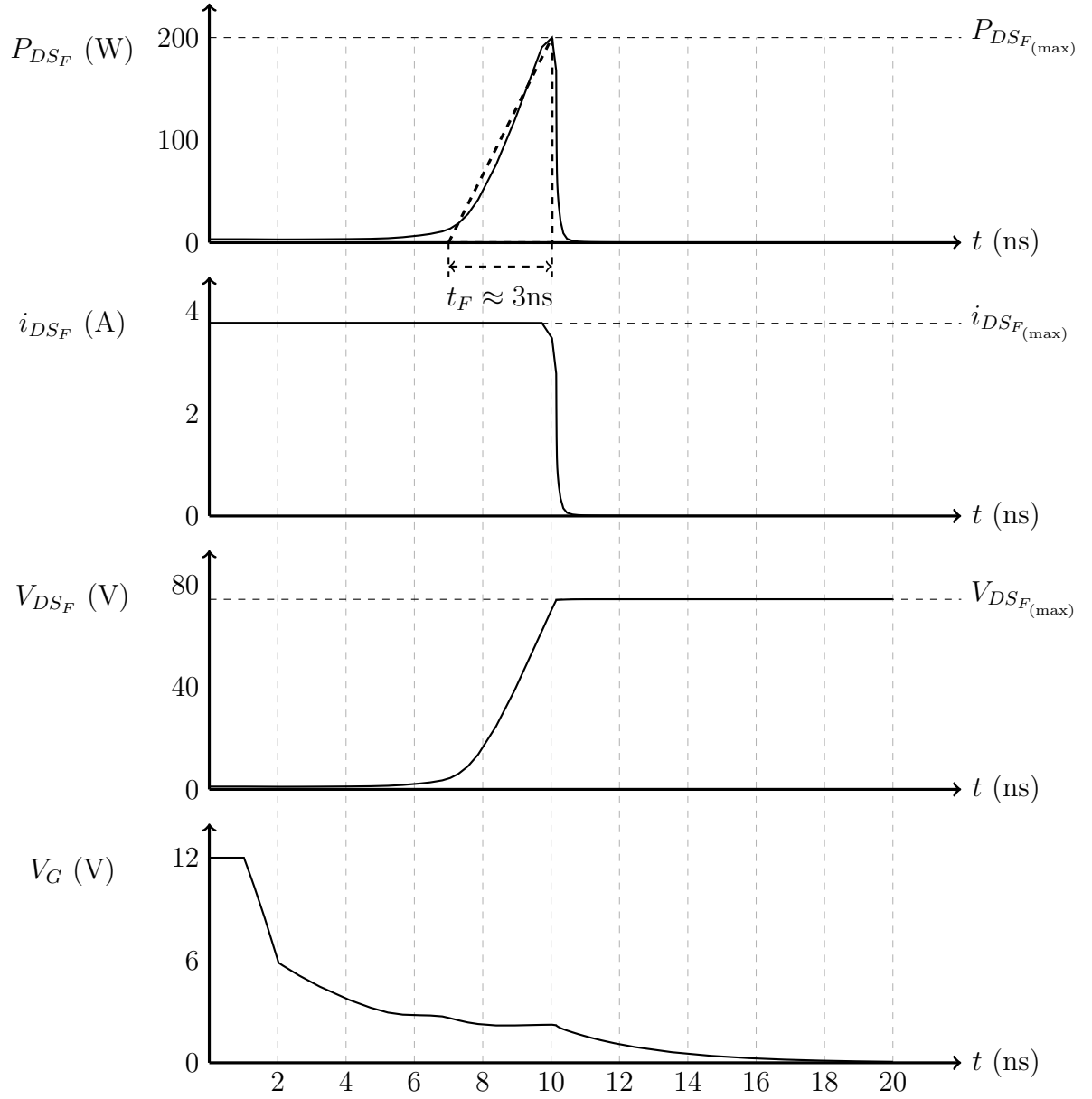


Fig. 3.13: MOSFET voltage, current and power waveforms during switch-off

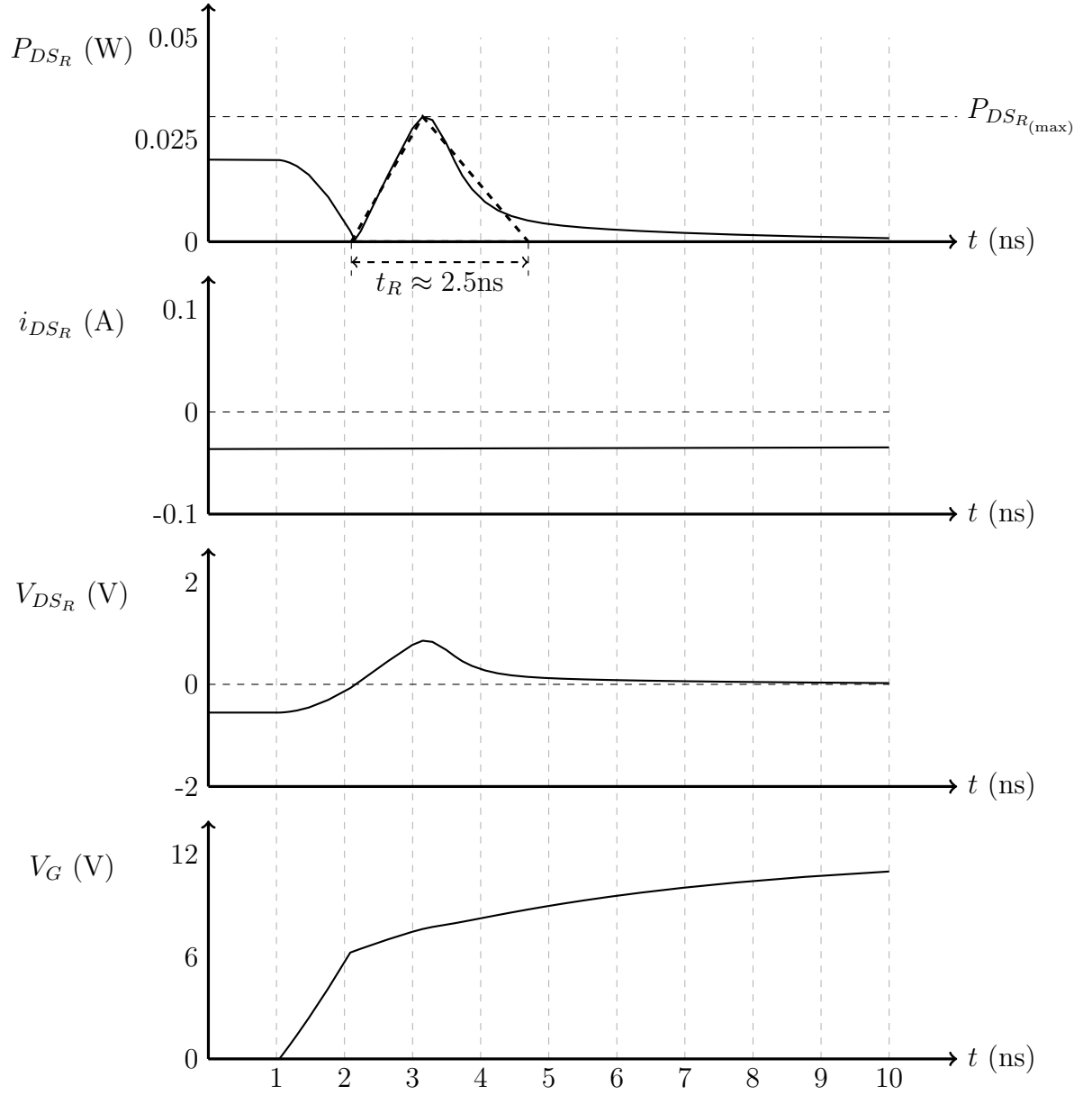


Fig. 3.14: MOSFET voltage, current and power waveforms during switch-on

The energy converted to heat in a single transition is given by integrating the power waveforms P_{DS_F} and P_{DS_R} over their respective transition periods t_F and t_R

$$E_{SW_F} = \int_0^{t_F} P_{DS_F} \cdot dt \quad (3.12)$$

$$E_{SW_R} = \int_0^{t_R} P_{DS_R} \cdot dt \quad (3.13)$$

These can be crudely approximated using straight-lines as shown in Figures 3.13 and 3.14 to give

$$E_{SW_F} \approx \frac{1}{2} t_F \times P_{DS_F(\max)} \approx 352 \text{ nJ} \quad (3.14)$$

$$E_{SW_R} \approx \frac{1}{2} t_R \times P_{DS_R(\max)} \approx 38 \text{ pJ} \quad (3.15)$$

Then the average power dissipation over a switching period T is then given as

$$P_{SW(\text{Avg})} = \frac{E_{SW_F} + E_{SW_R}}{T} = 0.03 \text{ W} \quad (3.16)$$

During steady state operation the power in the system should satisfy the equation

$$P_{in(\text{Avg})} - P_{out(\text{Avg})} - (2 \times P_{S(\text{Avg})}) - (2 \times P_{D(\text{Avg})}) - (2 \times P_{SW(\text{Avg})}) - P_{elec(\text{Avg})} - P_{mag(\text{Avg})} = 0$$

and using the values from (3.6), (3.9), (3.10), (3.11), (3.16) and Figure 3.4

$$138.7 - 124.2 - (2 \times 1.44) - (2 \times 0.423) - (2 \times 0.03) - 0.653214 - 7.38 = 2.68 \text{ W}$$

This equation shows that all sources of loss within the circuit have been identified and quantified. There is a small but inevitable error as measurements and manufacturer data will always have a degree of uncertainty. In this case it leaves 2.68W unaccounted for, giving an uncertainty of $\approx 7\%$ which can be attributed to measurement and rounding errors.

The total power loss in the circuit is given by

$$\text{Total Loss} = P_{in} - P_{out} = 138.7 - 124.2 = 14.5 \text{ W}$$

The proportion of power contributed by the magnetic assembly and MOSFETs is given by

$$\frac{P_{mag(Avg)} + (2 \times P_{S(Avg)}) + (2 \times P_{SW(Avg)})}{\text{Total Loss}} = \frac{7.38 + (2 \times 1.44) + (2 \times 0.03)}{14.5} = 0.7117$$

It can be shown from these values that the magnetic assembly and MOSFET switching/conduction contribute about 70% of the overall power loss. This is significant as the MOSFET losses are linked to the magnetic assembly as discussed in Section 4.0.2.

4. DISCUSSION

The Weinberg design has been adapted in the proposed topology for high conversion ratio boost applications making it a hybrid which combines non-isolated coupled inductor architecture with interleaved switching. Applying overlapped switching techniques removes the necessity for the presence of the “Discharge Path” which comprises of inductor $L_{1:2}$ and diode D_1 in Figure 1.41.

The proposed topology uses a non-isolated coupled inductor arrangement which is important for maintaining high efficiency. The coupled inductor system acts as an energy reservoir which is necessary to allow stable high voltage boosting. All coupled coils are wound on a common core in the same phase and consequently the flux flowing in the magnetic core does not reverse direction which reduces associated core losses. The input inductor is the driving force which transfers the energy through the circuit but does not bear full responsibility for magnetic energy storage. This allows the core losses to be spread between the two wound components.

The architecture of the coupled coils clamps the MOSFET drain voltage to an amount less than the output voltage (Figure 4.5) which allows lower breakdown voltage versions with inherently lower internal ON-resistance to be used. The output diodes conduct a relatively low current to that of the MOSFETs but consequently must block a much higher reverse voltage. A single capacitor exists on the output for smoothing.

4.0.1 Modes of Operation

The proposed topology has three distinct modes of operation as shown in Figure 4.1.

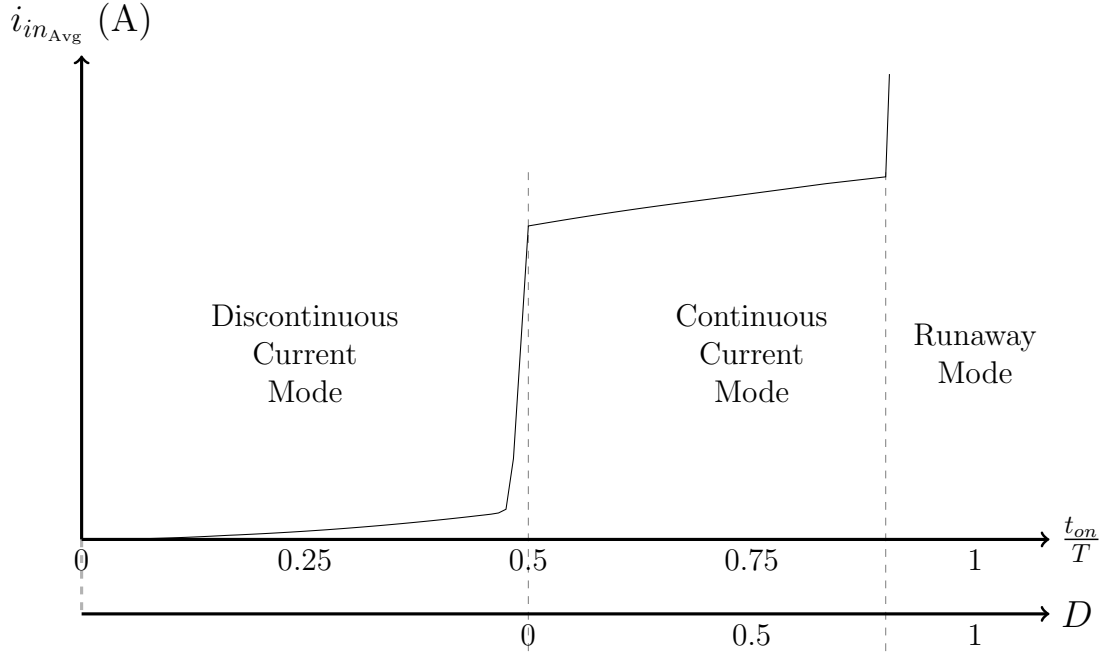


Fig. 4.1: Simulated input current against switch-on time

For each switch, t_{on} represents the time within a switch period T for which that switch is closed.

- Discontinuous Current Mode:

When $\frac{t_{on}}{T} < 0.5$ there is a period of time where both switches are open and no current path exists through L_{in} . This causes the current through L_{in} to fall to zero during this period.

- Continuous Current Mode:

When $\frac{t_{on}}{T} > 0.5$ the circuit operates in its normal mode. There is a linear relationship between the duty cycle D and the average input current.

- Runaway Mode:

When $\frac{t_{on}}{T}$ approaches unity there comes a point when $t_{(OV)} > (\frac{T}{2} - t_{(OP)})$ and subsequently $t_{(ID)} \leq 0$. If $t_{(ID)}$ is forced to or below zero the input inductor L_{in} cannot discharge sufficiently to maintain stable operation and will eventually saturate. If $\frac{t_{on}}{T} = 1$ the switch is closed 100% of the time. L_{in} will saturate and create a short circuit between the power supply and ground.

The lower bound for linear operation is fixed at $\frac{t_{on}}{T} = 0.5$, below which the circuit enters discontinuous current mode. The upper bound for linear operation

is variable dependent on $t_{(OP)}$. $t_{(OP)}$ expands as more power is passed through the circuit. As $t_{(OP)}$ increases, $t_{(ID)}$ decreases. $t_{(OV)}$ should be kept as small as possible for a given switching period T . While T can be dynamically adjusted to regulate power transfer, D should be kept constant at around $0.05 \rightarrow 0.1$ to allow $t_{(OP)}$ maximum possible expansion room. If $t_{(OP)}$ forces $t_{(ID)}$ to reduce to zero the circuit enters Runaway mode.

This is reflected in Figures .51,.52,.53,.54 where the circuit behaviour wildly diverges from the mathematical models.

When operating with an unregulated output voltage, the circuit follows its voltage transfer function (2.16)

$$\frac{V_{out}}{V_{in}} = (2 + \eta) \left(\frac{1}{1 - D} \right)$$

This comprises of two main variables, the duty cycle D , defined as the overlap to non overlap time ratio (2.9), and η which is the turns ratio of the coupled coils (2.13). This transfer function is made up of two sections which is the classic boost transfer function $\left(\frac{1}{1-D} \right)$ and a multiplying factor $(2 + \eta)$. This means the boost ratio follows the basic pattern of the classic boost converter which can be seen by comparing the plots in Figures 1.1b and 4.2a. This is repeated at higher levels as the multiplier η is increased. As η increases, it dominates the transfer function equation and has a larger effect on the boost ratio than the duty cycle. This allows higher boost ratios to be achieved with low duty cycles. The input current follows a curve proportional to the boost ratio which multiplies with increasing values of η as shown in Figure 4.2b. This means there is not a point where the circuit enters Runaway but excessive currents at high duty cycles are experienced just like with the classic boost topology.

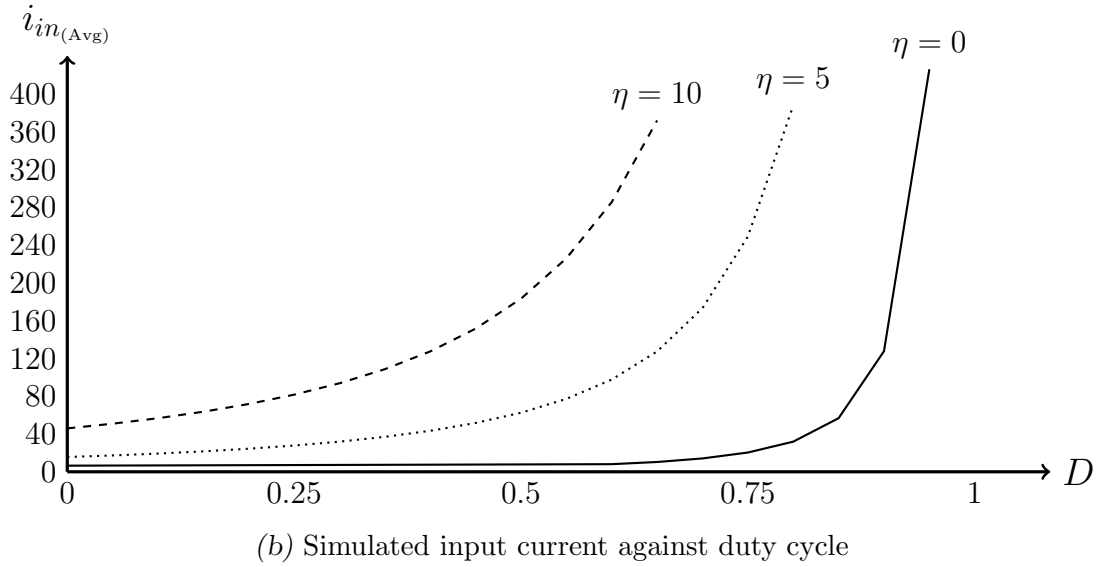
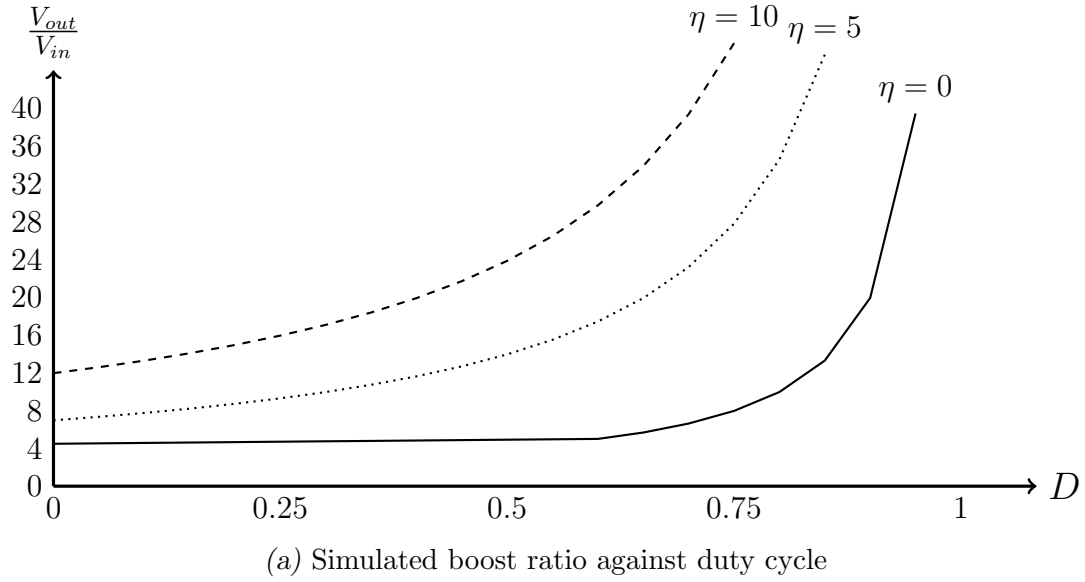


Fig. 4.2: Simulated boost ratio and input current against duty cycle when operating with an unregulated output voltage

When the output voltage is fixed the duty cycle has no effect on the boost ratio as shown in Figure 4.3a. Even if the input voltage is variable, the circuit will naturally adjust the boost ratio to suit. The power throughput is a function of the input voltage V_{in} and the switching period T as outlined in Section 2.0.3. There is a linear relationship between both T vs $i_{in(Avg)}$ and D vs $i_{in(Avg)}$ but T has a much more pronounced effect (Figures .46 and .51). Consideration should be made that η is not set too large as it causes $t_{(OP)}$ to expand and constrains the available power throughput capability. From Figure 4.3b the threshold at which the circuit enters Runaway occurs at lower duty cycle as η increases.

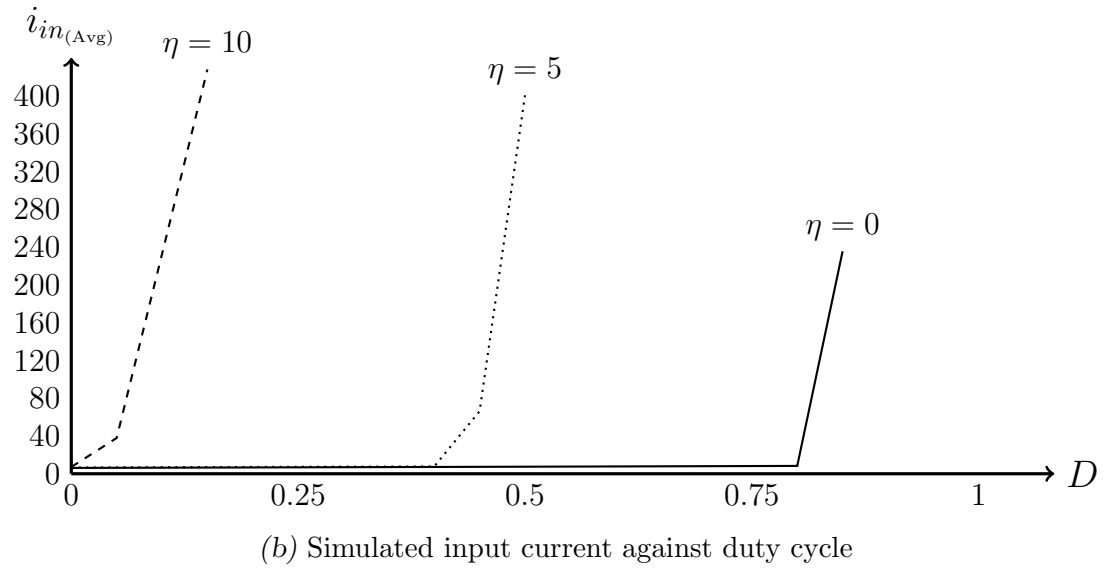
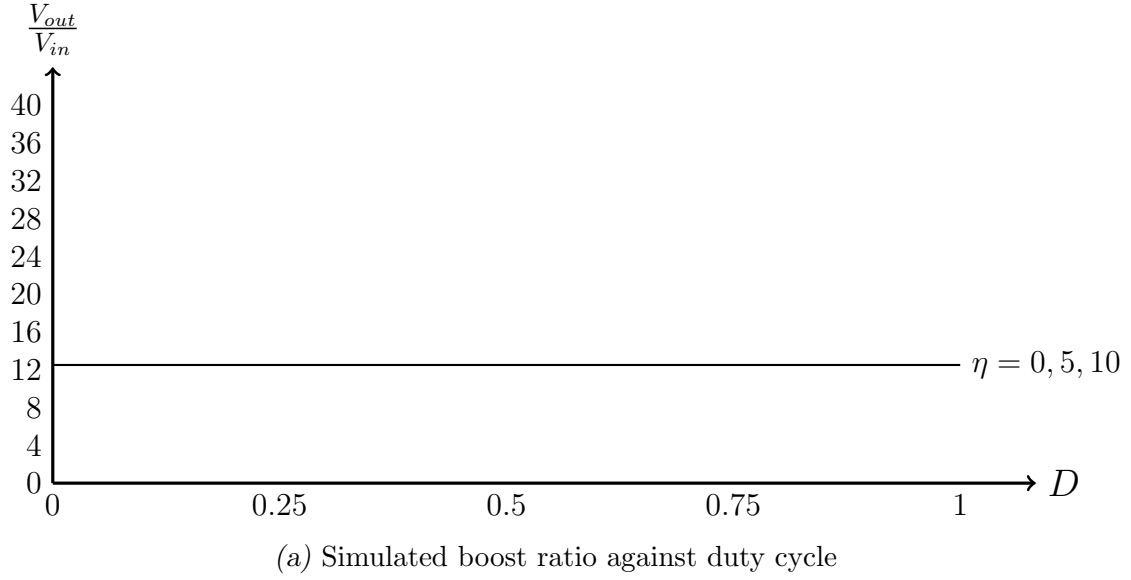


Fig. 4.3: Simulated boost ratio and input current against duty cycle when operating with a regulated output voltage

4.0.2 Prototyping

Three prototypes were constructed over the testing phase. The first prototype consisted of crudely wound magnetic coils on a simple toroidal core. It was expected to exhibit significant loss and so all external components were over-rated to ensure survival. MOSFETs with breakdown voltages of 1kV and diodes with reverse voltages of 1kV were employed. High voltage MOSFETs tend to have higher internal ON-resistance, 0.48Ω in this case. The efficiency of this first prototype was relatively poor at 89%. Large voltage spikes and high-frequency oscillations appeared on the MOSFET drains when operating at power levels above a few tens of Watts which would cause occasional failure due to over-voltage breakdown or over-heating. Loss analysis carried out in Section 3.0.1 showed that MOSFET switching loss was the second-highest contributor.

In the second prototype, diodes with reverse voltages of 600V and MOSFETs with breakdown voltages of 200V were substituted with a subsequently reduced ON-resistance of just $10\text{m}\Omega$. It was expected that the MOSFET losses would be reduced due to the lower ON-resistance. This prototype was operated at lower power levels to ensure component survival while loss observations were made. Efficiency did not improve and MOSFETs began to heat up significantly whenever attempts were made to operate at higher power levels. Some basic snubbing was applied to the MOSFETs to allow operation at higher power levels. As a result the MOSFETs did remain cool, instead the snubbing components became excessively hot. This proved that while the MOSFET was dissipating the power it was not the cause of the loss.

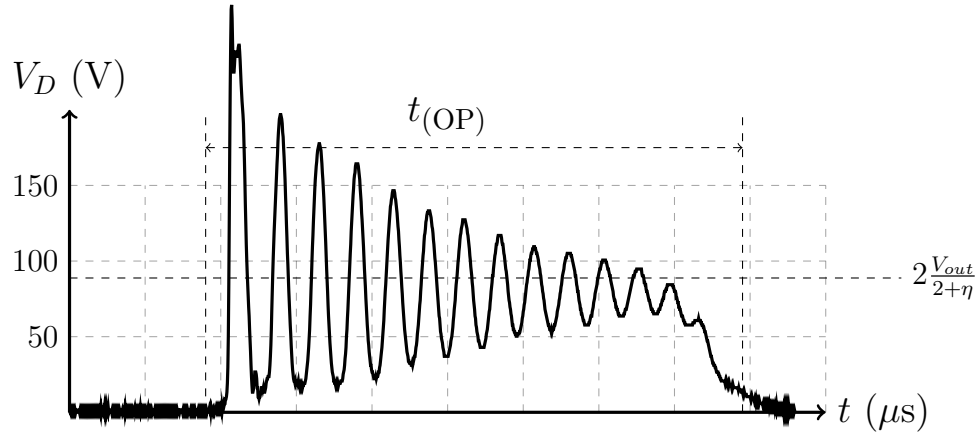
From the modelling performed in Section 3.0.1, it was found that the magnetic windings and material were the prime source of loss, both directly and indirectly. Poor magnetic coupling and increased leakage inductance create high frequency Eddy currents in the windings and material. This generates direct loss because if high frequency oscillating currents exist in the magnetic windings there will also be high frequency oscillations in the magnetic flux as can be seen in Figures 3.8 and 3.10. This causes increased power dissipation in the core material as shown in Figures 3.11 and 3.12.

This also generates indirect loss in the external components. As MOSFET switches tend to connect directly to the magnetic windings, there will be oscillating voltages on the MOSFET drains as shown in Figure 4.4a. These are sufficiently high in frequency to couple through the small intrinsic Gate-Drain capacitance in the MOSFET and the same oscillations appear on the Gate. This causes the MOSFET not to switch cleanly. It spends longer time periods in a semi-conductive state which dissipates more power internally and the MOSFET heats up.

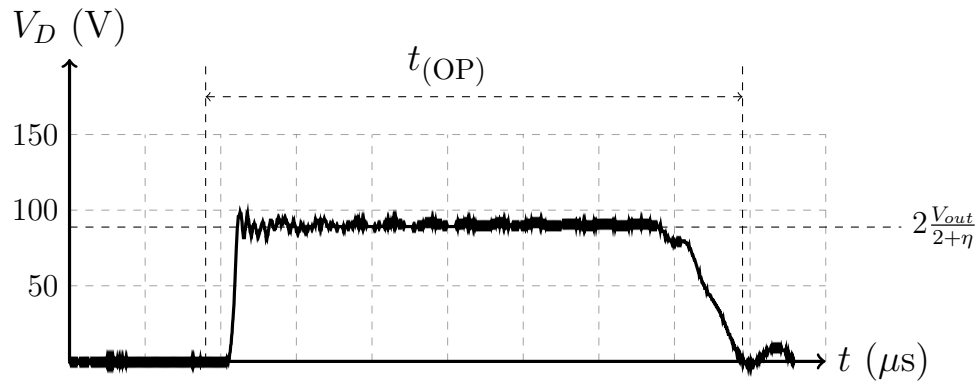
This is a known problem and snubbing is widely employed to resolve it. Correctly designed snubbing circuitry can alleviate these problems and maintain efficiencies

of well over 90%. However, it could be argued that snubbing does not solve the problem but simply goes around it. The source of the loss still exists but the waste energy is re-routed away from the switching components and recycled back into the circuit to allow high efficiency to be maintained. This comes at the cost of higher component count and the heightened risk of component failure leading to lower reliability.

The final prototype was upgraded with careful considerations made to the geometry of the magnetic material and windings. Specifically, the toroid core was replaced with a bobbin and air-gap to help store the magnetic energy more efficiently. Also the single core conductor was replaced with Litz wire to help reduce Eddy current generation and skin effect. The external components from the previous prototype were retained and all snubbing was removed. Oscillations from the magnetic coils were significantly reduced and the MOSFET switched much cleaner (Figure 4.4b) and MOSFET drain voltages clamp as expected (Figure 4.5).



(a) Low magnetic coupling factor, large leakage inductance



(b) High magnetic coupling factor, small leakage inductance

Fig. 4.4: MOSFET drain voltage waveform against magnetic assembly build quality
 $V_{out} = 250\text{V}$

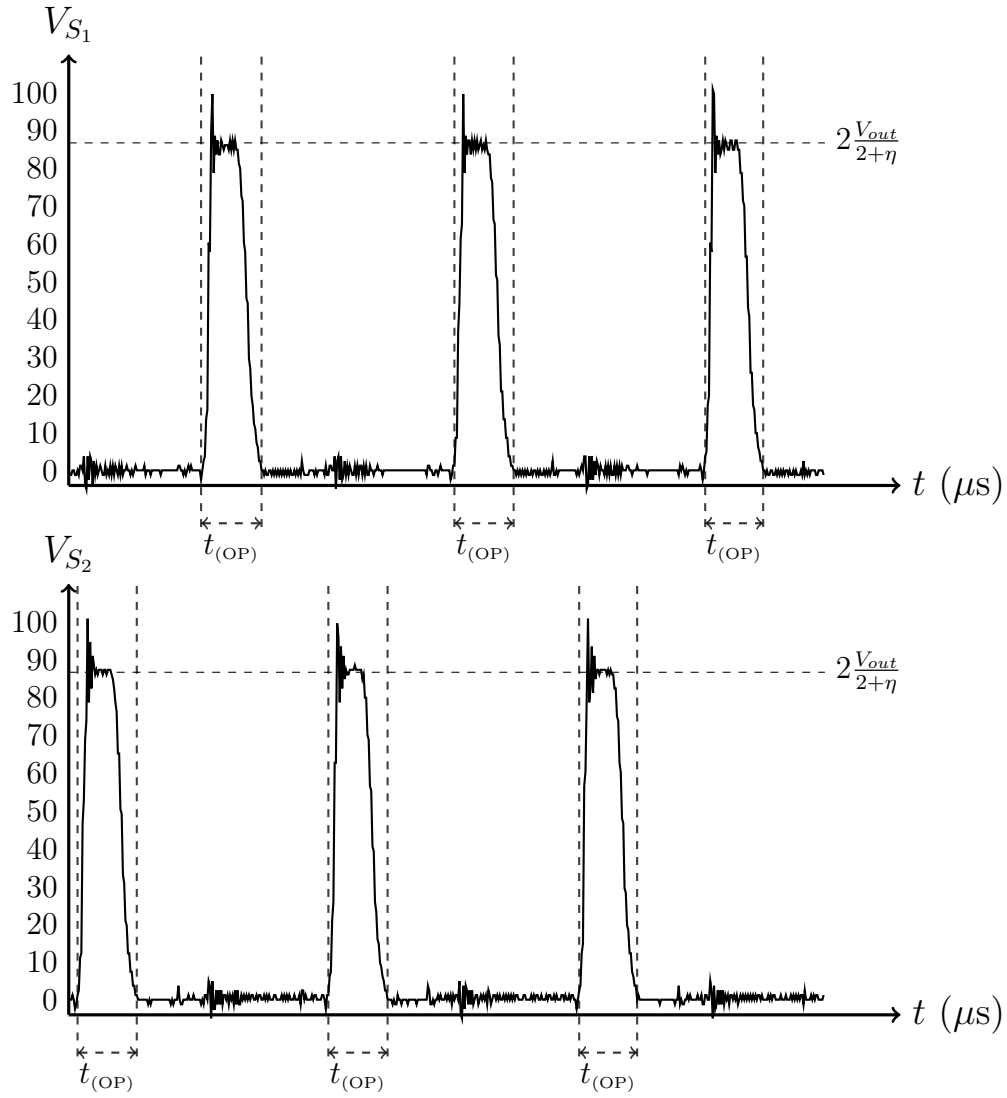


Fig. 4.5: MOSFET Drain voltage waveforms when $V_{out} = 250\text{V}$

The final prototype with the bobbin-wound magnetic assembly is shown in Figure 4.6 and all components used are laid out in Table 4.1.

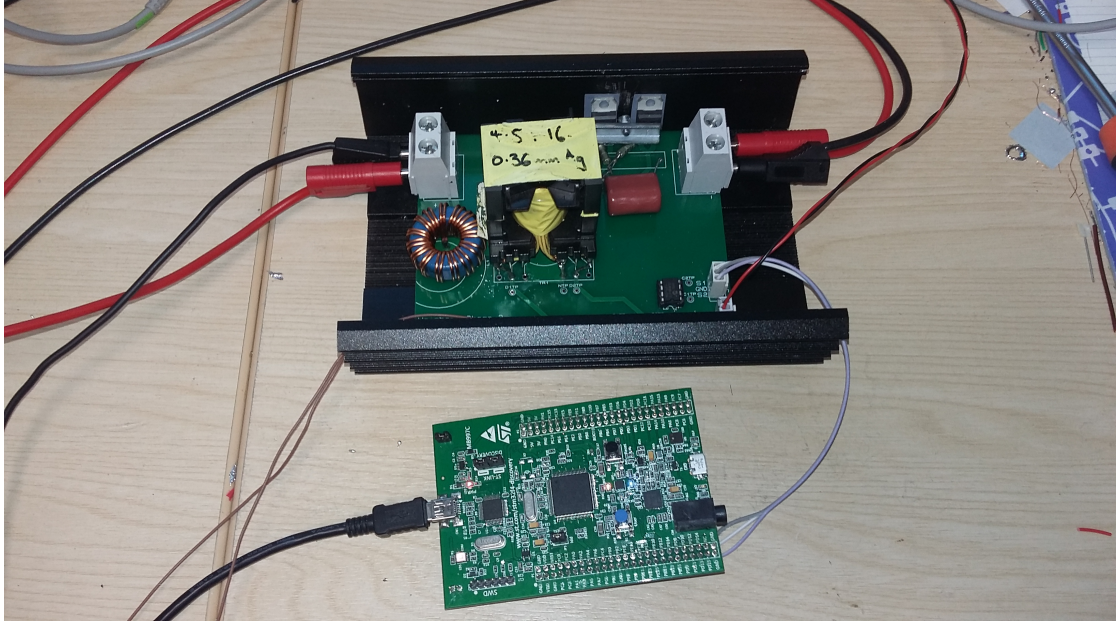


Fig. 4.6: Constant output voltage final prototype assembly with STM-Discovery switching control board

Component Label (from Figure 2.1)	Value/Part
L_{A1}/L_{A2}	10 μ H
L_{B1}/L_{B2}	130 μ H
L_{in}	36 μ H
C_{out}	4.7 μ F
S_1/S_2	IPP110N20N3 200V 88A Power MOSFET, $R_{DS(on)} = 10\text{m}\Omega$
D_1/D_2	STTH16R04 400V 16A Power Diode

Tab. 4.1: Constant output voltage final prototype assembly component list

Losses were reduced by half and efficiency increased to over 94% as shown in Figure 4.7. The prototype could operate comfortably at an output power of 257W without snubbing.

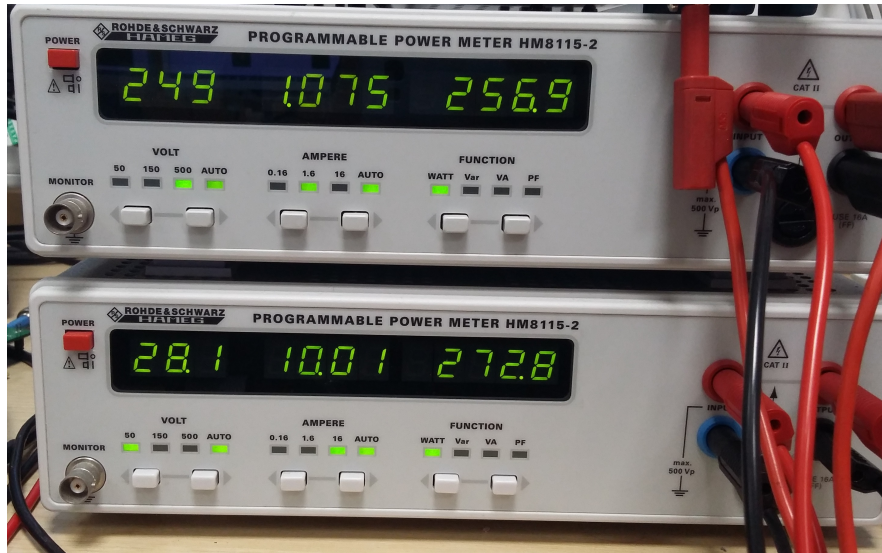


Fig. 4.7: Constant output voltage final prototype assembly power measurements
Bottom: Input power, Top: Output power.

Input Voltage:	28.1	V
Input Current:	10.01	A
Input Power:	272.8	W
Output Voltage:	249.0	V
Output Current:	1.075	A
Output Power:	256.9	W
Total Efficiency:	94.17	%
Boost Ratio:	8.86x	

While these results show that optimising the magnetic assembly can produce clean switching without snubbing, it is potentially much more involved than simple snubbing circuit design and possibly offers less tolerance to variation. This would mean precise machine winding would be necessary to replicate these positive results. From an ‘Ease-of-implementation’ standpoint, snubbing could be regarded as the more attractive option in some circumstances as it’s easily replicated after the initial design is sound. However, the magnetic assembly used in the final prototype was hand-wound and produced a favourable result. It’s likely that a machine-wound assembly would produce even better results.

Two final prototypes have been constructed to validate the operation of the proposed topology. One intended for PV cell Grid-Tie (micro-inverter) application which is a constant output voltage implementation (discussed above). It will boost the PV cell output, which is typically 35-45VDC, to 370VDC for injection into the UK mains grid. The output voltage is clamped by the load so the circuit does not control it but needs to be built such that it will tolerate such voltages.

The second is intended for non-constant output voltage application. It is currently under test feeding solar power into an electric space heater (Appendix .8) for renewable energy based home heating. The test system comprises of a single 300W PV cell which outputs typically 35-45VDC. The converter is designed to have a boost ratio of around 3x and boosts this voltage to around 100VDC which is then fed into the heater. A simple MPPT algorithm is implemented based on the voltage transfer function (2.16) to ensure the maximum power is always drawn from the PV cell.

4.0.3 Applications

The topology has application in renewable energy source interfacing to the power grid (grid-tie) and battery charging systems such as Kinetic Energy Recovery Systems (K.E.R.S.). The requirement here is to step up ELV DC to LV DC.

Renewable energy sources are dependant on a wide variety of naturally occurring and highly changeable conditions. Modern day demands for renewable energy are complex, with the requirement to attempt maximum power extraction from renewable sources under these conditions. Renewable energy source locations are often dispersed and inaccessible. Located in isolated places makes monitoring of their variable power more difficult and almost always has to be done remotely. Maintenance and other human intervention is also difficult. Robust but simple construction is key as minimal complexity means lower chance of failure. These situations have led to a rising trend for “Fit-and-Forget” installations which can be relied on to operate faultlessly for extended time periods without any human intervention. Examples of this include Satellites, Deep-sea oil extraction systems, and high demand services which require fluent operation and where serious disruption

can result from a failure such as road/rail signalling systems, Air Traffic Control and other fundamental services.

4.0.4 Maximum Power Point Tracking (MPPT) Applications with Constant Input and Output Voltages

From simulation and experiment the input power, input voltage and switching period are linearly related . This is verified in the simulation results provided in Appendix .7, Figures .46 and .36, where the average input current is linearly related to the switching period T and input voltage V_{in} . The average input current can be converted to the average input power by multiplying with the input voltage V_{in} . From Figure .41 the output voltage has a very small effect on the input power where a variation of several hundred volts only creates an input current variation of about 0.5A.

From the simulation results provided in Appendix .7 the effects of the variable circuit parameters on the average input current can be approximated as follows

$$\begin{aligned} i_{in(Avg)}(V_{in}) &\approx 0.25 \left(\frac{A}{V} \right) \\ i_{in(Avg)}(V_{out}) &\approx 0.0005 \left(\frac{A}{V} \right) \\ i_{in(Avg)}(T) &\approx 0.75 \left(\frac{A}{\mu s} \right) \\ i_{in(Avg)}(D) &\approx 0.012 \left(\frac{A}{\%} \right) \end{aligned}$$

These values apply with the circuit parameters given in Appendix .7, they will be different with other parameter values. The input voltage V_{in} and switching period T are clearly dominant thus the input power as a function of variable circuit parameters can follow the rough relationship

$$P_{in} = kTV_{in} \text{ or } P_{in} \propto TV_{in}$$

where k simply stands in for all other circuit parameters; both constant and variable.

For MPPT applications this relationship can be applied such that the input voltage is measured and the switching period adjusted to set the power to a pre-determined value. Alternatively if the maximum power is unquantified then the instantaneous power can be quantified using the above relationship and the switching period can be adjusted until a maximum is reached.

4.0.5 How It Compares

The Conventional Interleaved converter (Section 1.0.5) is basically the classic boost topology replicated in parallel in order to handle higher currents. Interleaved switching can then be applied to increase the frequency of the ripple and smooth the input current waveform. Then replacing the singular inductor with a coupled inductor allowed larger boost capability as well (Section 1.0.8). The interleaved topology (Section 1.0.10) was a natural next step where the two parallel paths are inter-connected, either using diodes or magnetic coupling. Many interleaved converters, including the Weinberg, are closely related to the Coupled Inductor and Conventional Interleaved converters. Although varied at an individual level they still operate based on the same principles. Therefore this proposal bears a resemblance to some existing interleaved topologies such as those presented in [10,19,70,71] and of course the Weinberg itself [1] from which the proposed topology is derived.

Specifically there is a strong similarity with the proposed family of DC-DC converters in [19, 102]. The main differences are that instead of two coupled inductor assembly's there is one main magnetic system with a separate inductor at the input. All coupled windings are wound on a single magnetic core which allows the flux in both the inductor and coupled inductor system to run in continuous mode. The flux never falls to zero and never reverses direction which aids with reducing magnetic losses.

5. CONCLUSIONS

A.H. Weinberg presented his classic topology in his 1974 publication intended for use in satellites. It comprises minimal external components and uses multiple coupled magnetic systems to provide a boost of up to 2x. This thesis introduces a novel topology based on the Weinberg design and adapts it for high-boost operation.

An analysis of the proposed topology has been provided and mathematical expressions are derived to quantify the voltages and currents in salient components for a given set of operating conditions. The circuit can operate with both variable and fixed output voltages making it suitable for applications such as power feeding (Grid-Tie) and battery charging for electric vehicles. It follows a simple transfer function in both cases but significant limitations exist which must be considered in design to avoid non-linear behaviour.

From experimentation magnetic material and MOSFET conduction losses were found to contribute around 70% of the total circuit loss. Modelling and trialling of magnetic system geometries has been carried out to optimise magnetic coupling and reduce leakage inductance. All coupled windings share a single core and have been arranged so the magnetic flux does not reverse direction which further reduced loss in the magnetic core material. The coupled coils clamp the MOSFET drain voltage to an amount much lower than the output voltage which allows lower breakdown versions with lower intrinsic ON-resistance to be used leading to reduced conduction losses. The output diodes pass a relatively low current due to the relatively high output voltage which reduces their contribution to loss. The output current ripple is relatively low due to the overlapped switching which reduces the ESR related loss from the output smoothing capacitor. Upgrading from a toroidal core to a bobbin wound core with an air gap allowed the magnetic energy to be stored more efficiently in the fringing field. Additional protective components such as snubbers were not necessary. Overall, the proposed topology consists of a magnetic assembly, four windings on a common core, with two diodes, two MOSFET switches, one inductor and one low value output capacitor serving as the only external components.

Working prototypes have been developed and used to verify the mathematical claims through experimentation. Overall system efficiency of 94.1% has been achieved at a boost ratio of 8.8x and an output power of 257W. Overall system

losses were reduced from 11% to 6% by simply optimising the magnetic assembly. The results suggest that efforts may be better spent optimising the magnetic system as associated losses in external components are automatically reduced by extension. However optimisation of the magnetic assembly is more involved and may be less tolerant to variation which may hinder repeatability but the results are very positive despite crude, hand-wound magnetic coils and standard quality silicon components being used; which is a promising sign. It would be a fair assumption that better results would be possible if further care was taken in component selection and commercially produced magnetic assemblies were used.

6. FUTURE WORK

The analysis presented in this thesis assumes ideal conditions. The circuit exhibits slightly different behaviour under non-ideal conditions.

This section outlines some easily observable differences in circuit behaviour with non-ideal components in order to form the foundation of further analysis.

6.0.1 Analysis using Non-Ideal Components

Specifically non-ideal switches have $R_{off} < \infty\Omega$ and $R_{on} > 0\Omega$ and observable state-transition times. If N-channel MOSFETs are used there are intrinsic reverse-bias diodes which will allow reverse current to flow when the MOSFET is open. The coil in series with the open MOSFET induces a reverse current which previously was unable to flow with ideal switch models. This changes the model outlined in Sections 2.0.2 and 2.0.3. The modified equivalent circuits over the switching periods are shown in Figure 6.1 where intrinsic component losses are shown.

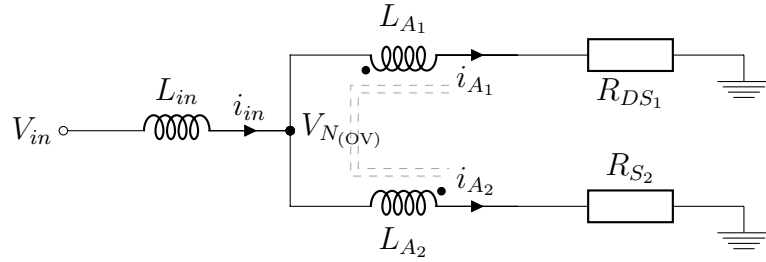
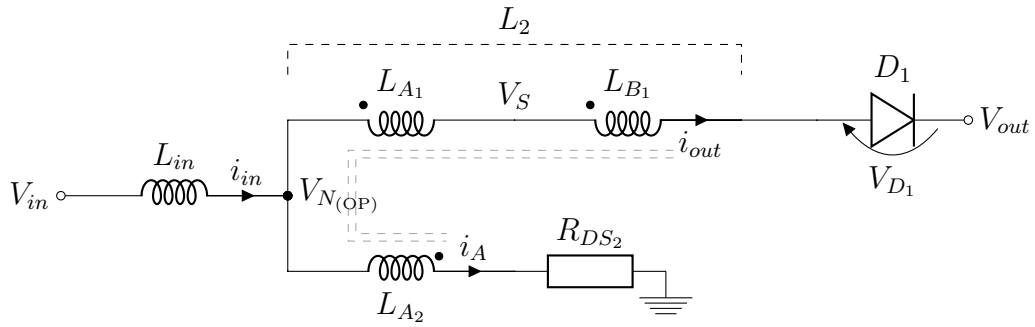
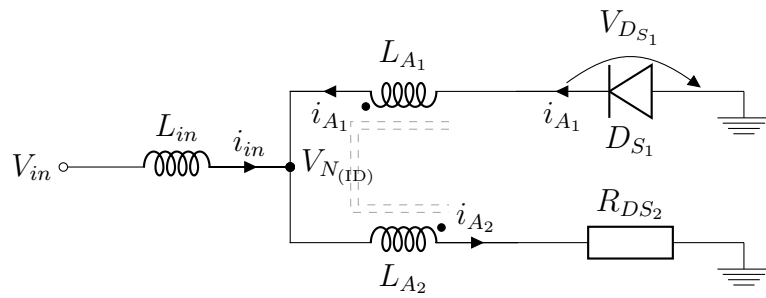
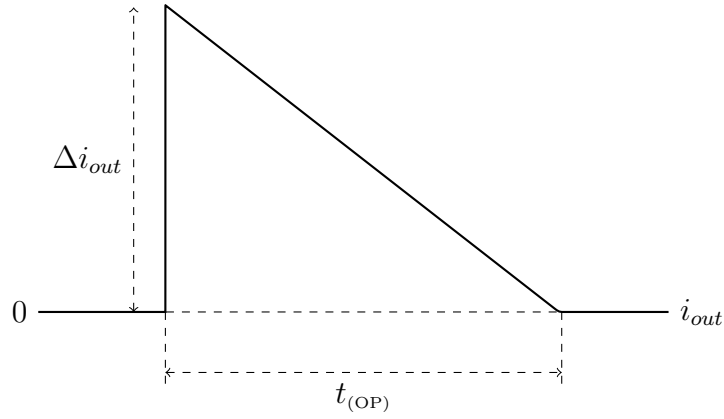
(a) Non-ideal equivalent circuit during $t_{(OV)}$ (b) Non-Ideal equivalent circuit during $t_{(OP)}$ (c) Non-Ideal equivalent circuit during $t_{(ID)}$

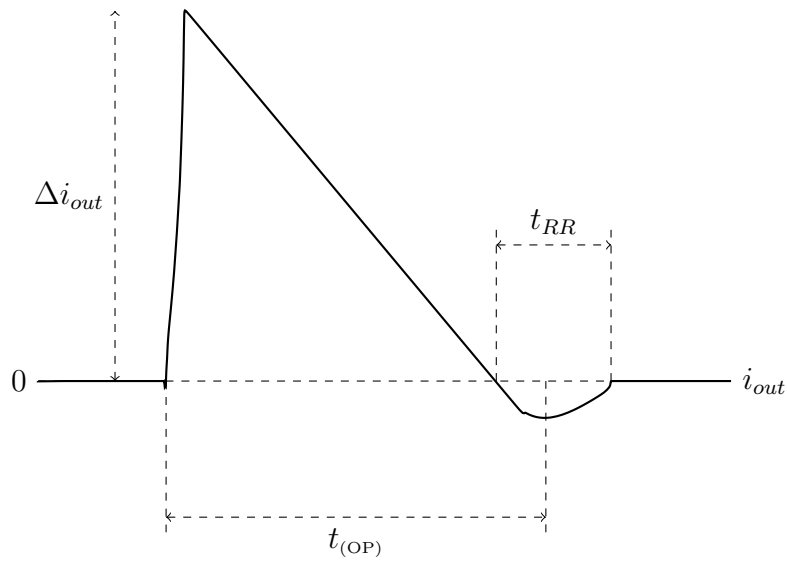
Fig. 6.1

Non-ideal diodes do not switch off instantaneously. There is a measurable reverse recovery and switch-off time as shown in Figure 6.2.

This affects the currents in the rest of the circuit as shown in Figure 6.3.



(a) Ideal diode response passing output current



(b) Real diode response passing output current

t_{RR} is the diode switch-off/reverse recovery time and is usually quantified on the diode data sheet.

Fig. 6.2: Ideal vs real diode responses using actual simulation data

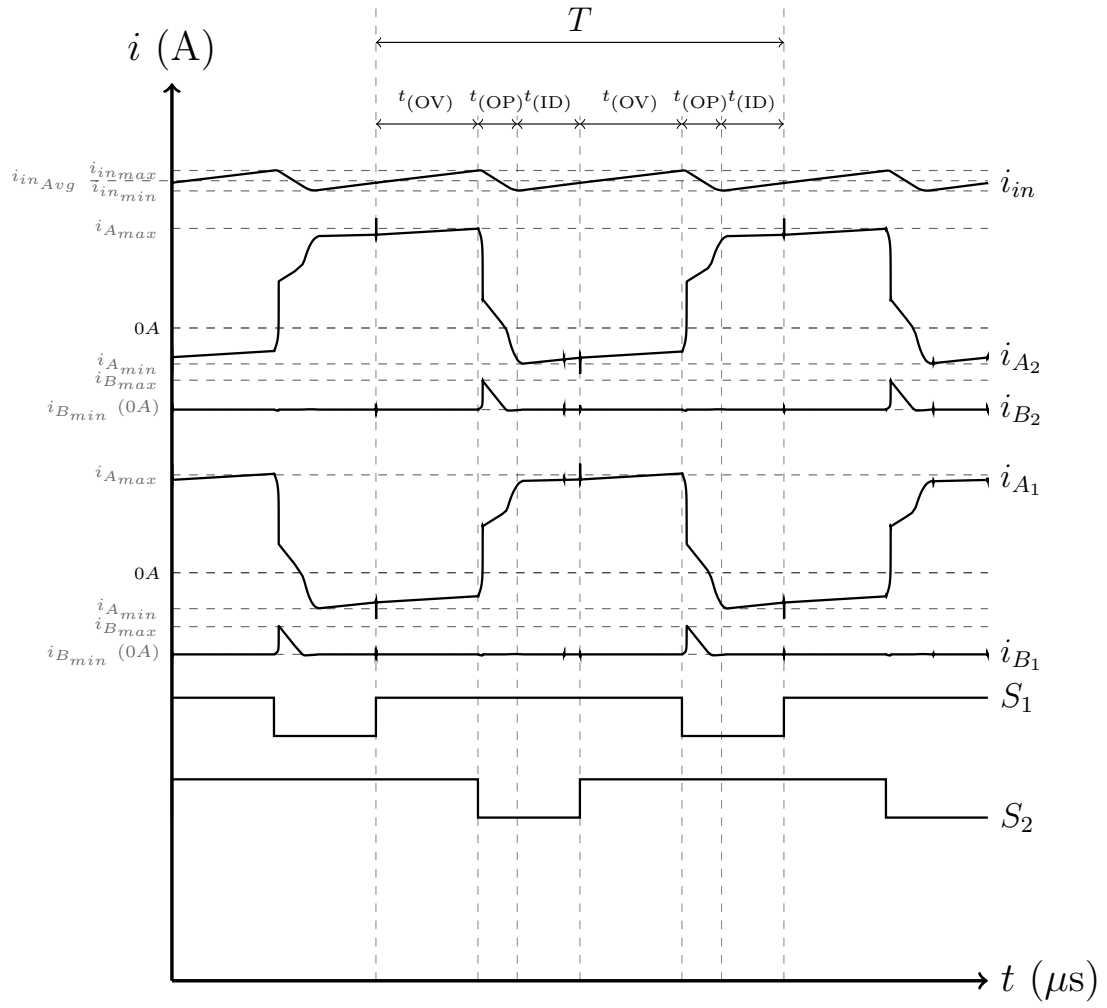


Fig. 6.3: Current waveforms for all coils using non-ideal components and simulation data

The effects of the intrinsic MOSFET diodes can be seen in Figure 6.3 where the current in L_{A_1} and L_{A_2} are now able to dip negative during $t_{(\text{ID})}$ and $t_{(\text{OV})}$. This is shown in greater detail in Figure 6.4 where g represents the magnitude of the afore mentioned negative dip. Note also that both i_{A_1} and i_{A_2} experience the same shift of magnitude g . When the one current dips negative the other jumps positive by the same amount due to (2.23), also shown in Figure 6.4.

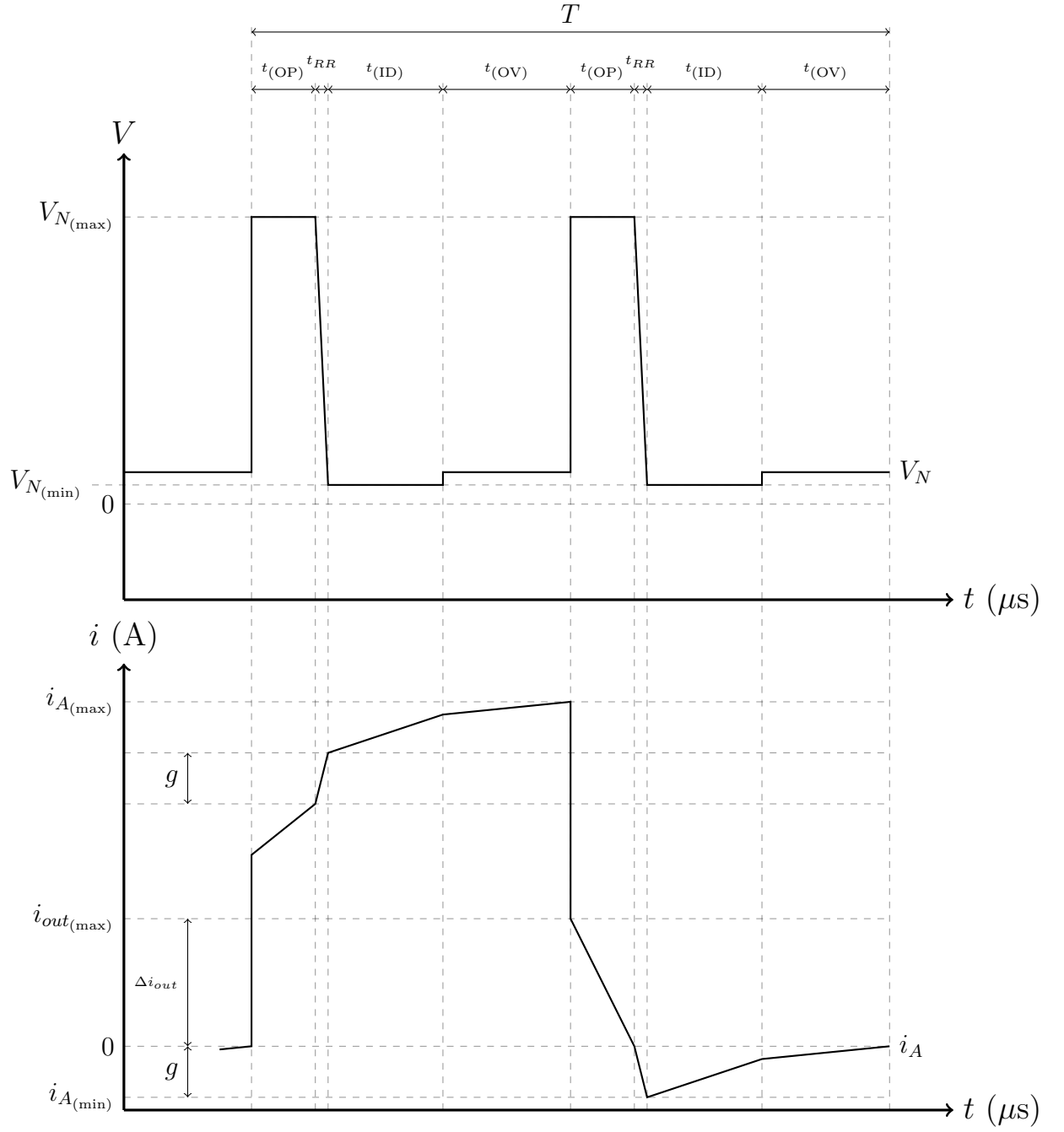


Fig. 6.4: Expanded transformer current and voltage waveforms using non-ideal components

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Appendices

.1 Glossary of Terms and Abbreviations

.1.1 Acronyms

Term	Definition
AC	Alternating Current
AC-DC Converter	A circuit used to convert an AC voltage to a DC voltage (E.g. Rectifier)
DC	Direct Current
DC-AC Converter	A circuit used to convert a DC voltage to an AC voltage (E.g. Inverter)
DC-DC Converter	A circuit used to convert one DC voltage to another DC voltage
ELV	Extra-low Voltage (voltages below 50VDC)
ESR	Equivalent Series Resistance - The internal resistance associated with capacitors which contributes to loss
K.E.R.S.	Kinetic Energy Recovery Systems - recovering energy from moving bodies via a dynamo such as Regenerative Braking
LV	Voltages between 50VDC (35.355Vrms) and 1kVDC (707.1Vrms) such as that used on the mains grid
MPPT	Maximum-Power-Point-Tracking
PELV	Protected ELV (voltages below 50VDC which may not be electrically isolated from the mains supply but include earth protection on the output)
SELV	Separated ELV (voltages below 50VDC which are electrically isolated from the mains supply)
VAC	AC-Volts - the voltage present on a specified node in an AC system, usually expressed in RMS Volts (Vrms)
VDC	DC-Volts - the voltage present on a specified node in a DC system

.1.2 Electrical Component Identifiers

Term	Definition
FET	Field Effect Transistor
High-Side	An arrangement of switching circuit where the FET connects the switched node to the supply
LED	Light Emitting Diode
Low-Side	An arrangement of switching circuit where the FET connects the switched node to ground
MOSFET	Metal-Oxide Semiconductor FET

.1.3 Electrical Mathematical Symbols

Term	Definition
C	Capacitor component identifier in circuit schematics or Capacitance term in equations (unit: Farad (F))
D	Diode component identifier in circuit schematics
i	Current (unit: Amps (A))
i_{DS}	FET Drain-to-Source current
i_D	FET Drain current
i_G	FET Gate current
i_S	FET Source current
i_x	Current through a component specified by x
L	Inductor component identifier in circuit schematics or Inductance term in equations (unit: Henry (H))
R	Resistor component identifier in circuit schematics or Resistance term in equations (unit: Ohm (Ω))
R_{DS}	Generic FET Drain-to-Source resistance
R_{off}	Switched-Off FET Drain-to-Source resistance
R_{on}	Switched-On FET Drain-to-Source resistance
SW or S	Switch or FET component identifier in circuit schematics
V	Voltage (unit: Volt (V))
V_{DS}	FET Drain-to-Source voltage (or blocking voltage)
V_{GS}	FET Gate-to-Source (or Switch-on) voltage
V_D	FET Drain voltage
V_G	FET Gate voltage
V_S	FET Source voltage
V_x	Voltage across a component specified by x

.1.4 Magnetics Mathematical Symbols

Term	Definition
μ	Overall permeability of a magnetic system ($\mu_0 \times \mu_r$)
μ_0	Permeability of Free Space ($4\pi \times 10^{-7}$)
μ_r	Relative permeability of a magnetic material
Φ	Magnetic flux (unit: Tesla (T) or Gauss (G _S))
A	Cross-sectional area of a magnetic flux path (unit: square meters m ²)
B	Magnetic Flux Density (unit: Tesla (T) or Webbers per square meter $\frac{\text{Wb}}{\text{m}^2}$)
H	Magnetic Field Strength (unit: Amps per meter $\frac{\text{A}}{\text{m}}$)
L	Inductance (unit: Henry (H))
l	Magnetic flux path length (unit: meters (m))
L_T	Total inductance of two mutually coupled inductors
M	Mutual inductance of two coupled inductors
N	Number of complete turns which make up an inductive coil

.1.5 General Mathematical Symbols

Term	Definition
Δi	Change in current (unit: Amps (A))
Δi_x	Change in current through a component specified by x (unit: Amps (A))
Δt	Time period or change in time (unit: seconds (s))
t	Time (unit: seconds (s))
T	Time for one complete switching cycle (unit: seconds (s))
G _S	Gauss (unit of magnetic flux density where 1G _S = 10 ⁴ T)

.2 *LTSpice Simulation Schematics*

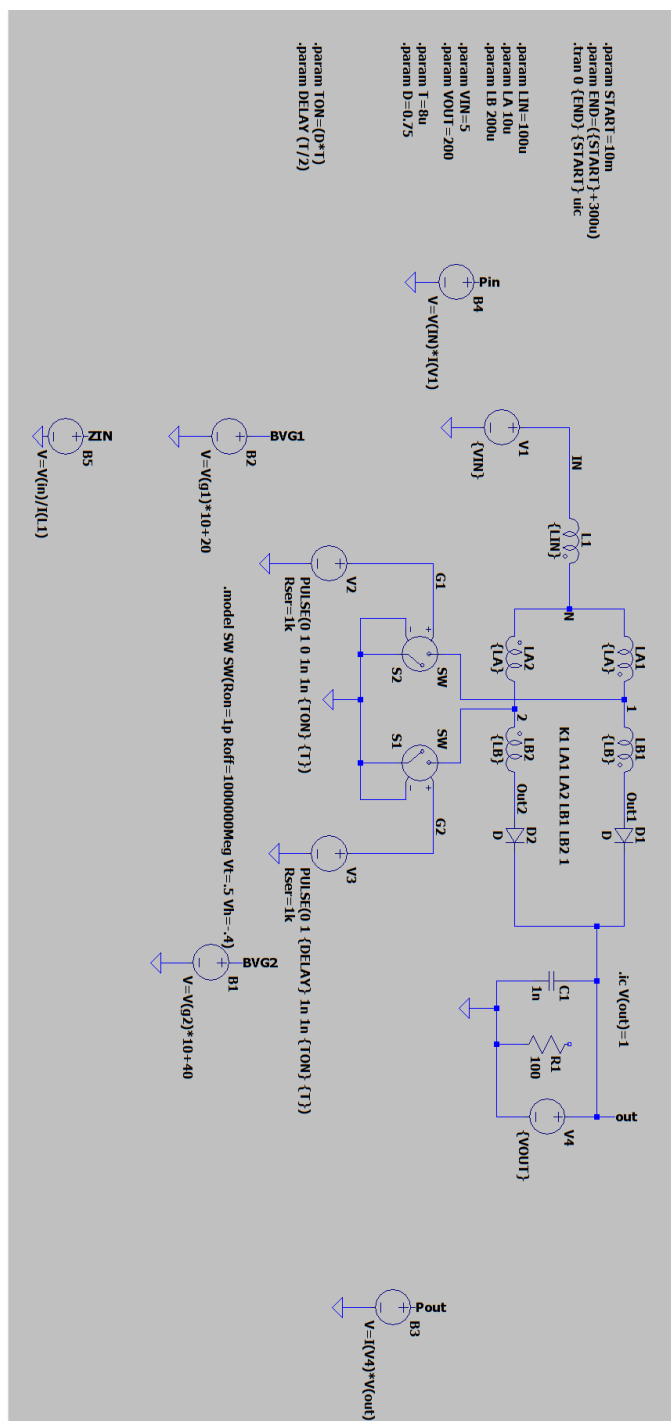


Fig. .5: LTSpice simulation schematic with ideal components and no losses

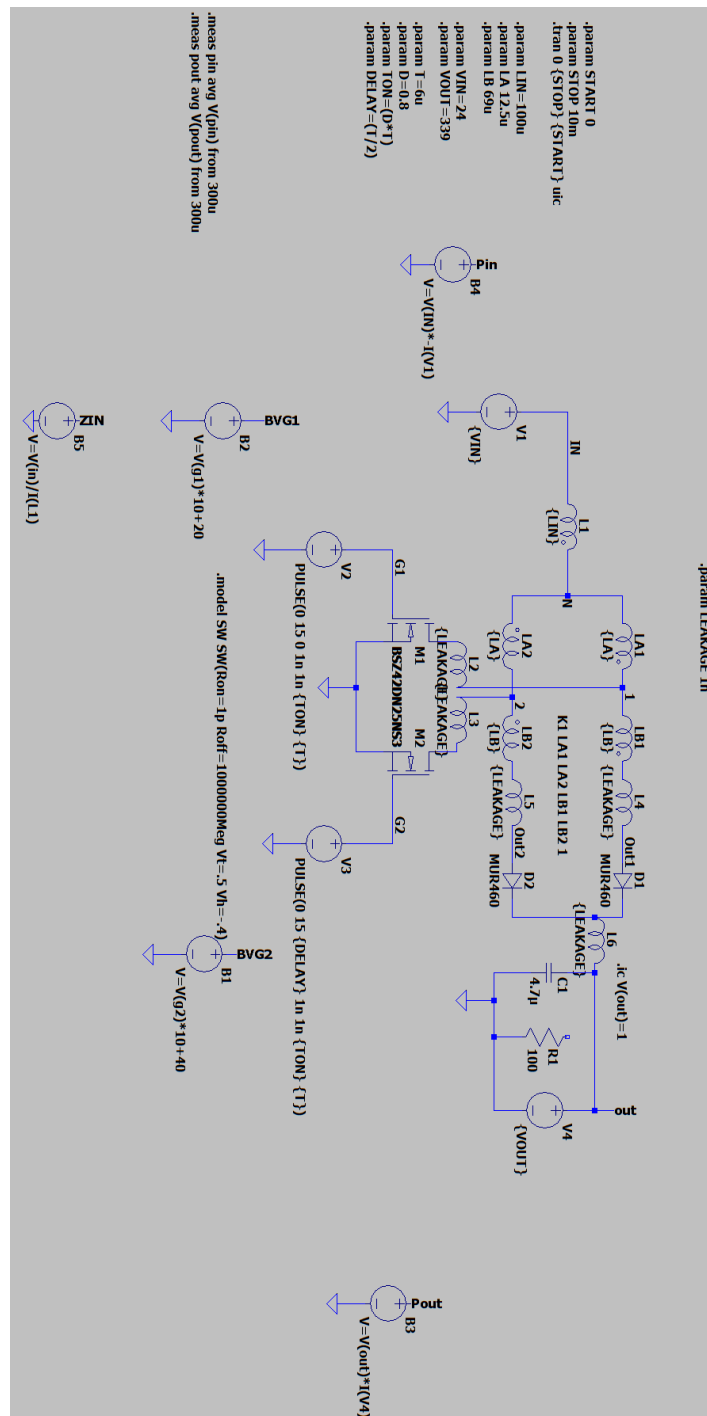


Fig. .6: LTSpice simulation schematic with non-ideal components, losses and leakage inductances included

3.3 Control Circuit Schematic

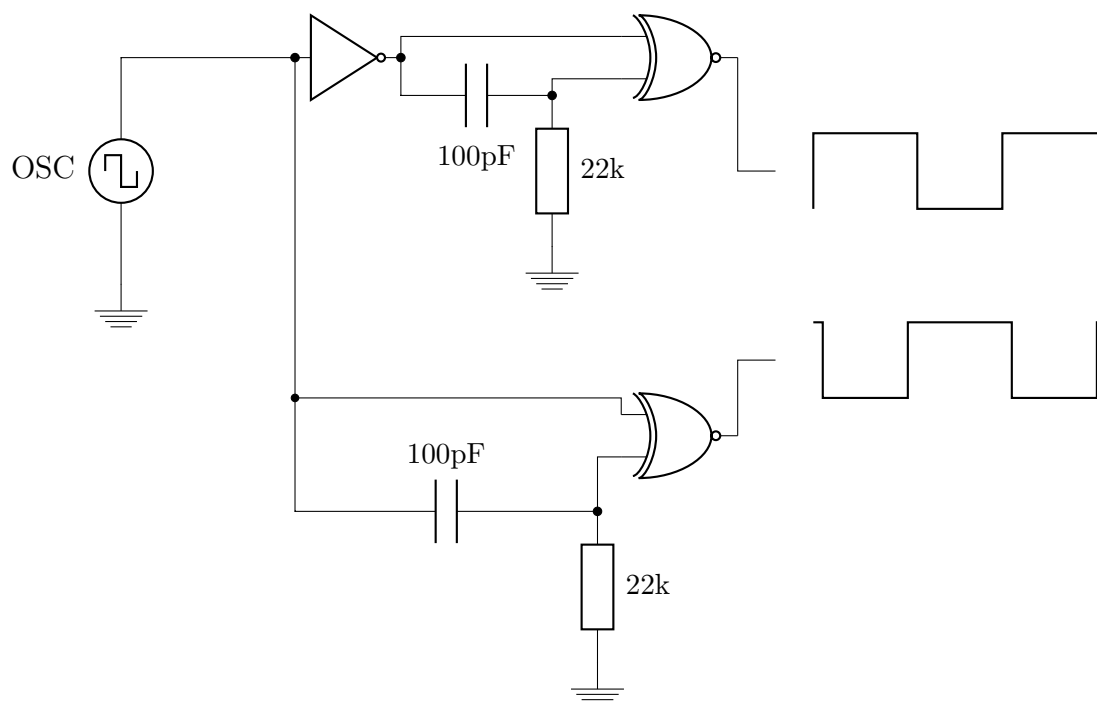


Fig. .7: Control circuit schematic with static dead time

.4 Magnetic core material characterisation



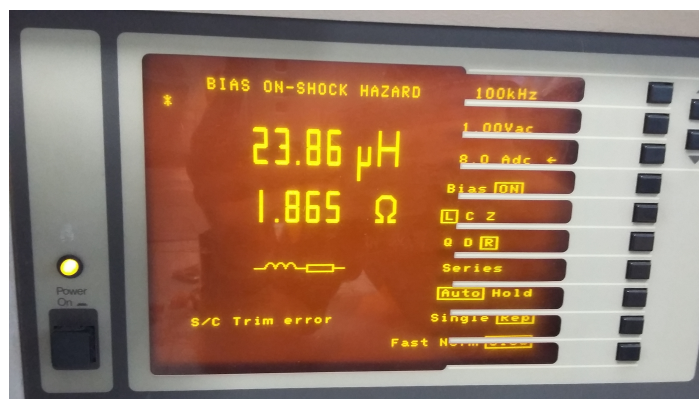
Fig. .8: Magnetic core measurement assembly
using Wayne-Kerr 3245 precision inductance analyser and Wayne-Kerr 3220 20A bias unit



(a) Measurement connection

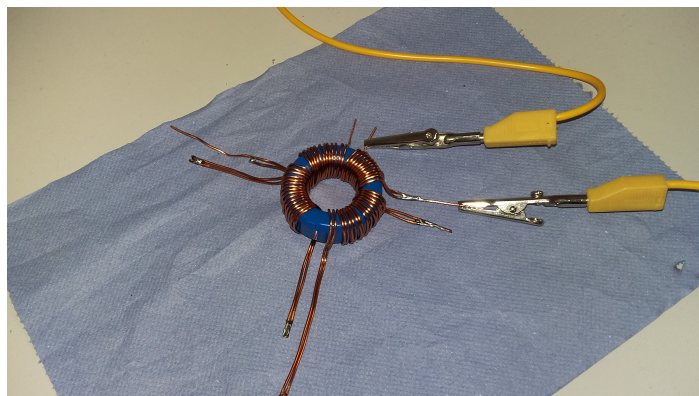


(b) No DC bias current



(c) 8A DC bias current

Fig. .9: Sendust MS-106125-2 characterisation



(a) Measurement connection



(b) No DC bias current



(c) 9A DC bias current

Fig. .10: Sendust MS-157125-2 characterisation

.5 *Fourier Analysis of Inductor Currents*

This section shows the FFT plots the data from which is used for quantifying electrical and magnetic losses in Section 3.0.2,3.0.3. The following parameters are used

$$L_{in} = 100 \mu\text{H} \quad (29 \text{ turns})$$

$$L_A = 20 \mu\text{H} \quad (10 \text{ turns})$$

$$L_B = 80 \mu\text{H} \quad (20 \text{ turns})$$

$$V_{in} = 32 \text{ V}$$

$$V_{out} = 150 \text{ V}$$

$$T = 10 \mu\text{s}$$

$$D = 0.1$$

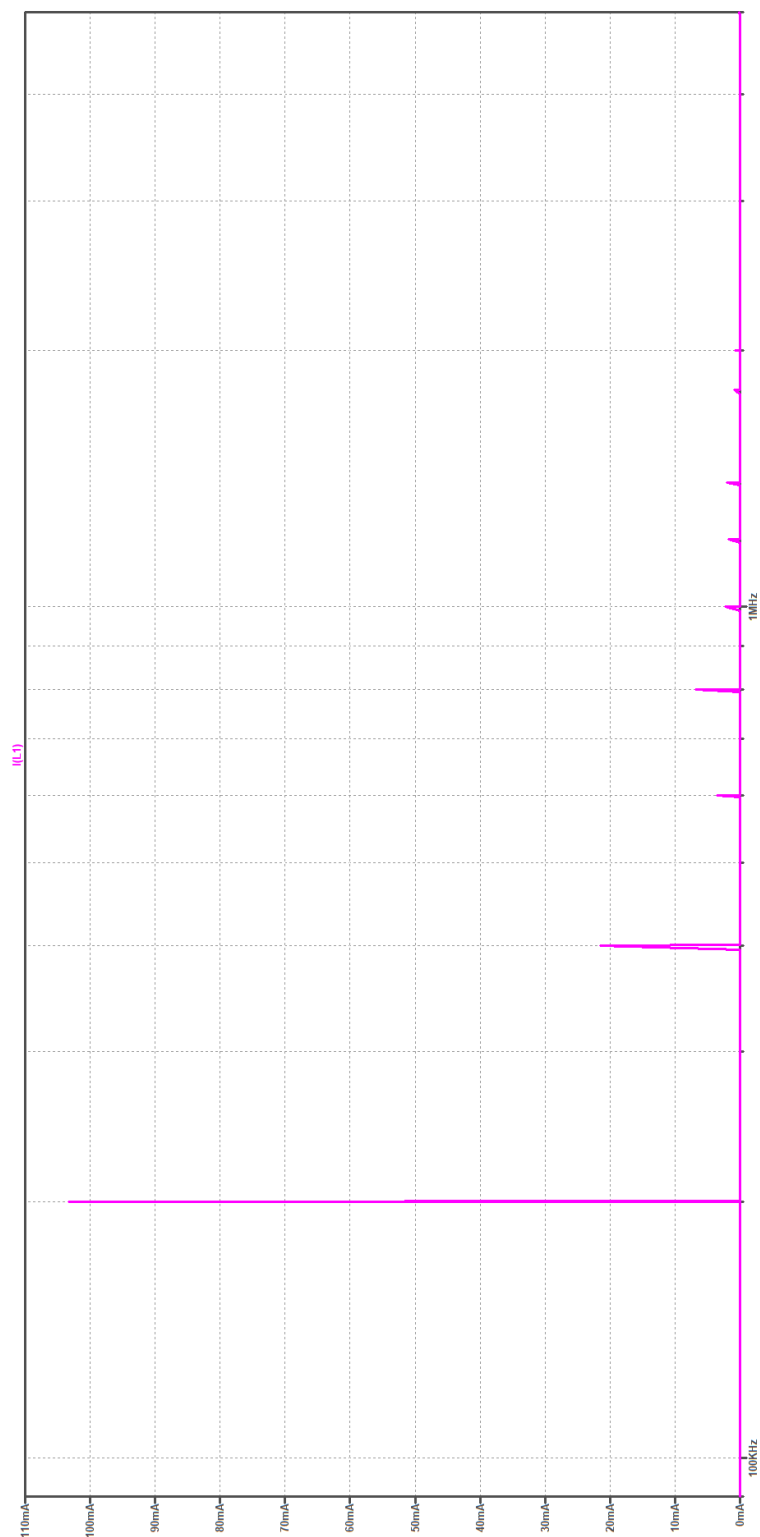


Fig. .11: FFT of simulated current $i_{L_{in}}$

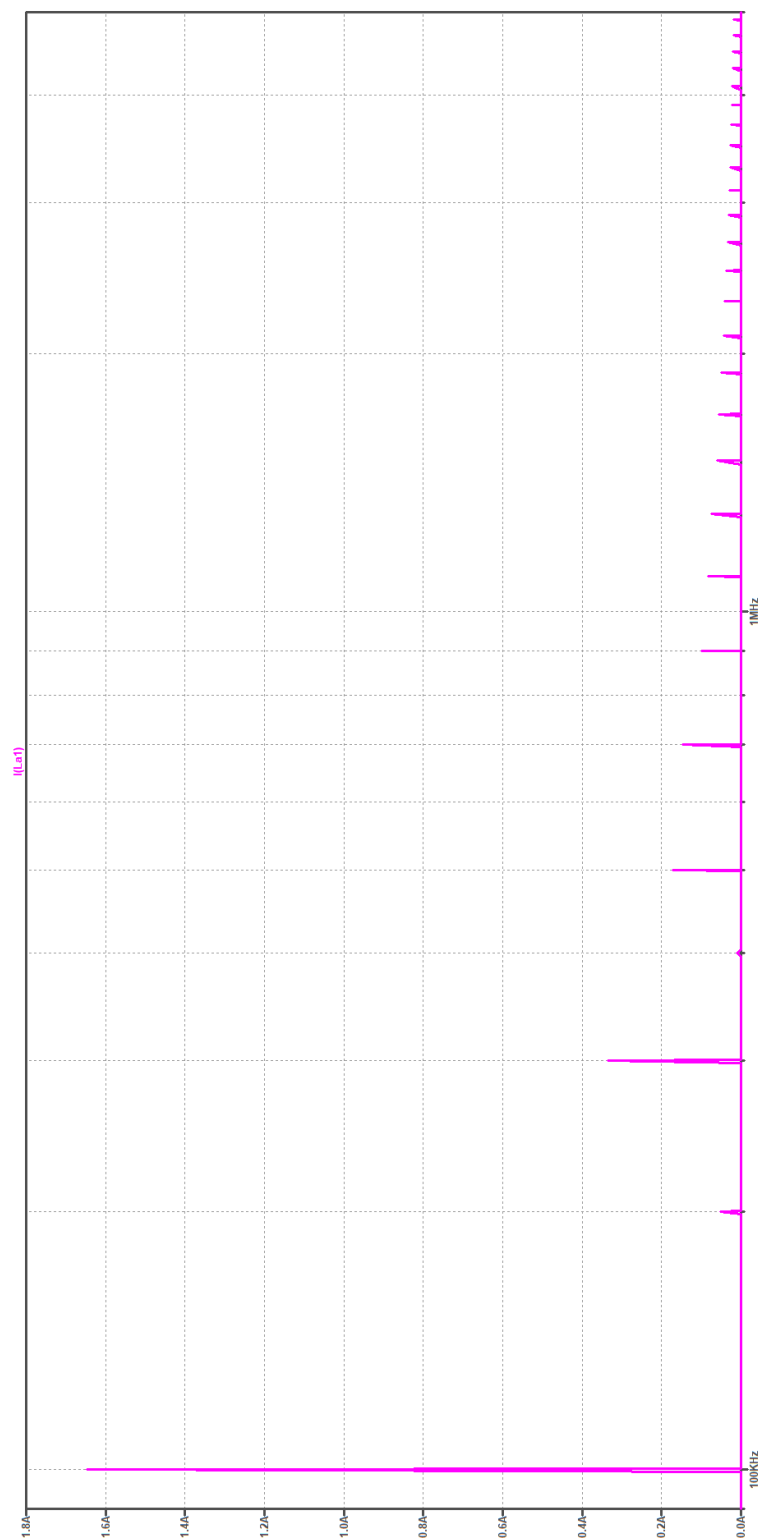


Fig. .12: FFT of simulated current i_{L_A}

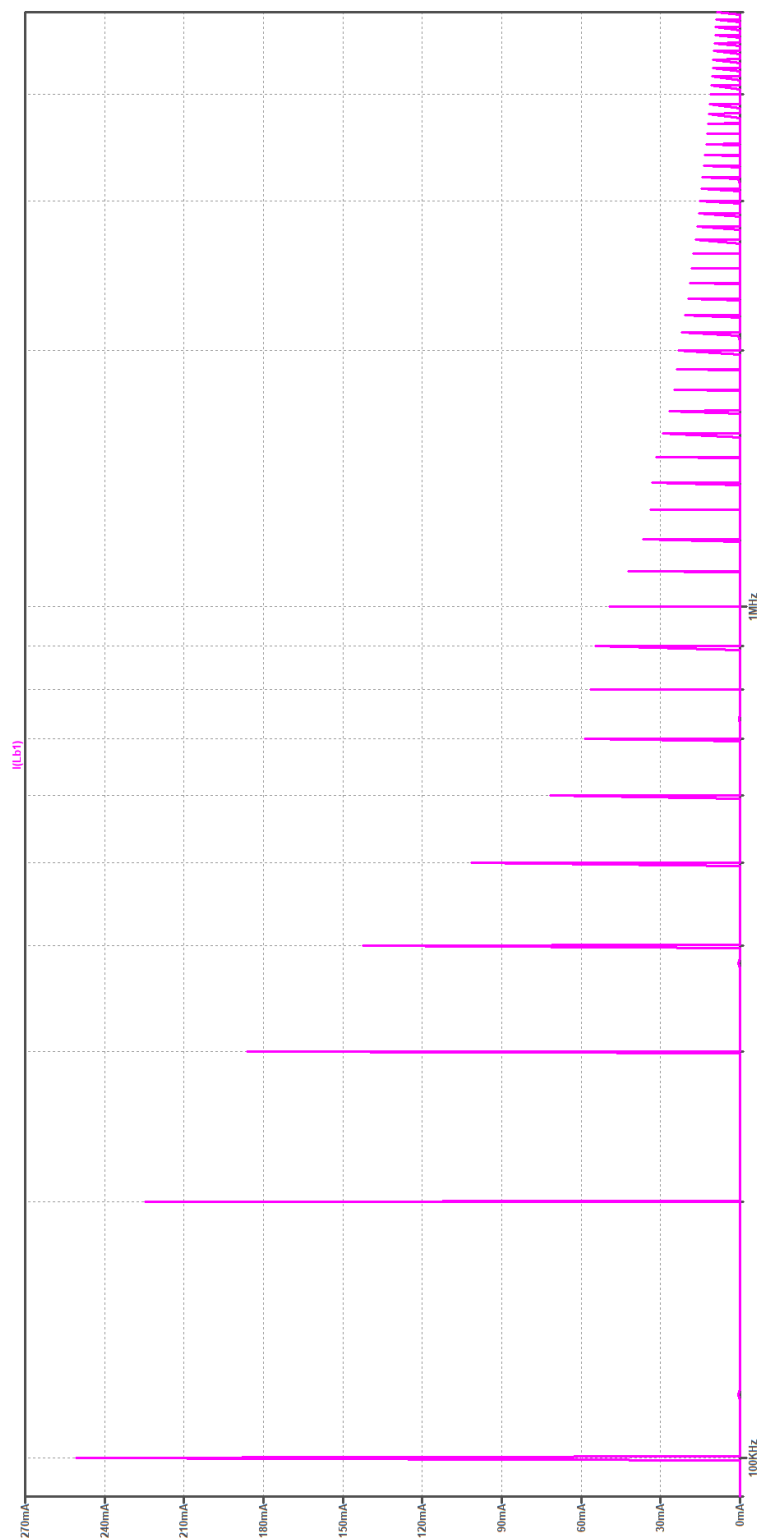


Fig. .13: FFT of simulated current i_{LB}

Frequency (kHz)	$i_{n(L_{in})}$ (A)	$i_{n(L_A)}$ (A)	$i_{n(L_B)}$ (A)
0	4.040	2.020	0.429
100	0.000	1.226	0.497
200	0.061	0.031	0.265
300	0.000	0.338	0.133
400	0.026	0.013	0.122
500	0.000	0.185	0.084
600	0.013	0.007	0.073
700	0.000	0.121	0.062
800	0.007	0.003	0.050
900	0.000	0.088	0.047
1000	0.003	0.001	0.038
1100	0.000	0.068	0.035
1200	0.001	0.000	0.030
1300	0.000	0.055	0.027
1400	0.001	0.000	0.025
1500	0.000	0.044	0.022
1600	0.001	0.000	0.020
1700	0.000	0.036	0.018
1800	0.001	0.000	0.016
1900	0.000	0.030	0.015
2000	0.001	0.000	0.013
2100	0.000	0.025	0.012
2200	0.000	0.000	0.011
2300	0.000	0.020	0.010
2400	0.000	0.000	0.009
2500	0.000	0.017	0.009
2600	0.000	0.000	0.008
2700	0.000	0.014	0.007
2800	0.000	0.000	0.007
2900	0.000	0.012	0.006
3000	0.000	0.000	0.006

Tab. .1: Magnetic winding current magnitudes over N_h harmonics

.6 Simulations for Non-Constant Output Voltage Operation

In this section the voltage transfer function derived in Section 2.0.2 is compared against simulation data.

The output voltage V_{out} as a function of circuit parameters is given by the voltage transfer function as

$$V_{out} = V_{in} \frac{2 + \eta}{1 - D}$$

The following base parameters are used

$$L_{in} = 100\mu\text{H}$$

$$L_A = 10\mu\text{H}$$

$$L_B = 80\mu\text{H}$$

$$V_{in} = 32\text{V}$$

$$T = 10\mu\text{s}$$

$$D = 0.1$$

In the following plots the circuit parameters maintain these values while a single parameter is swept across a range and the output voltage V_{out} is measured in each case.

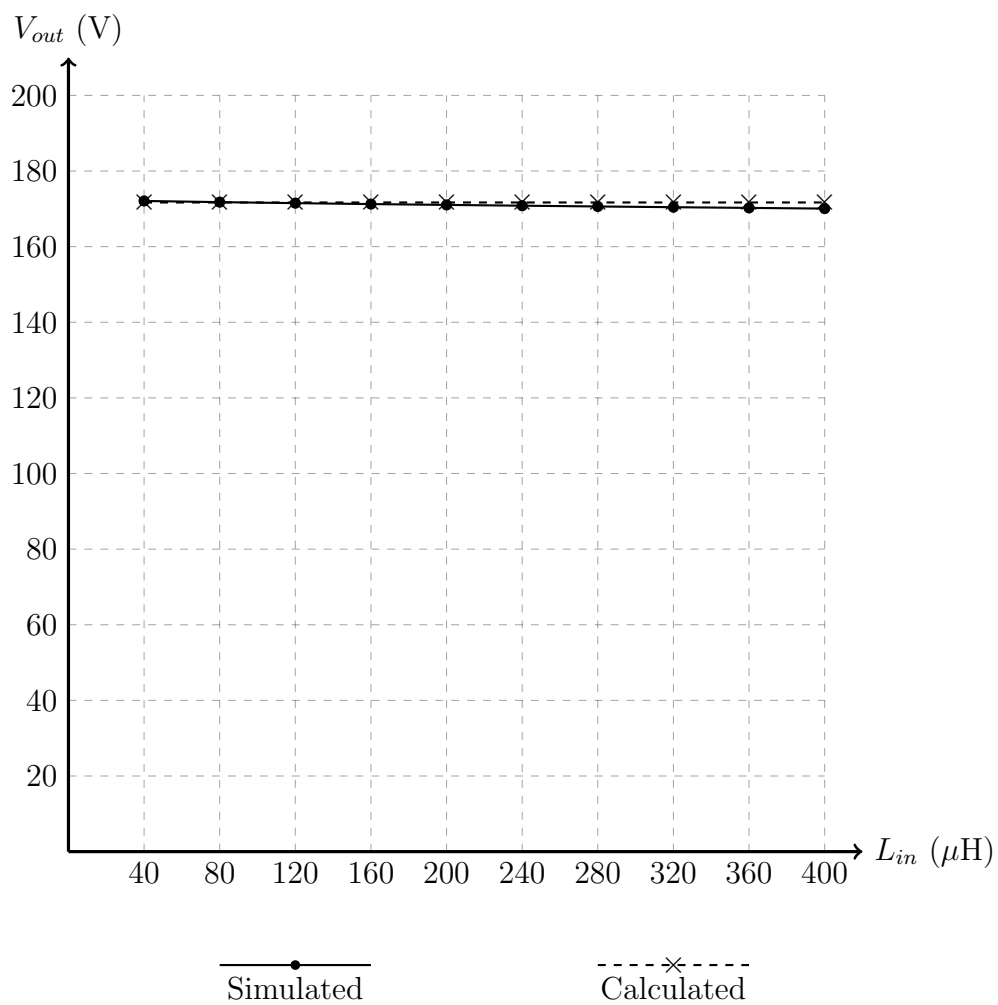


Fig. .14: Simulated vs calculated results for V_{out} while sweeping parameter L_{in} from $40\mu\text{H}$ to $400\mu\text{H}$

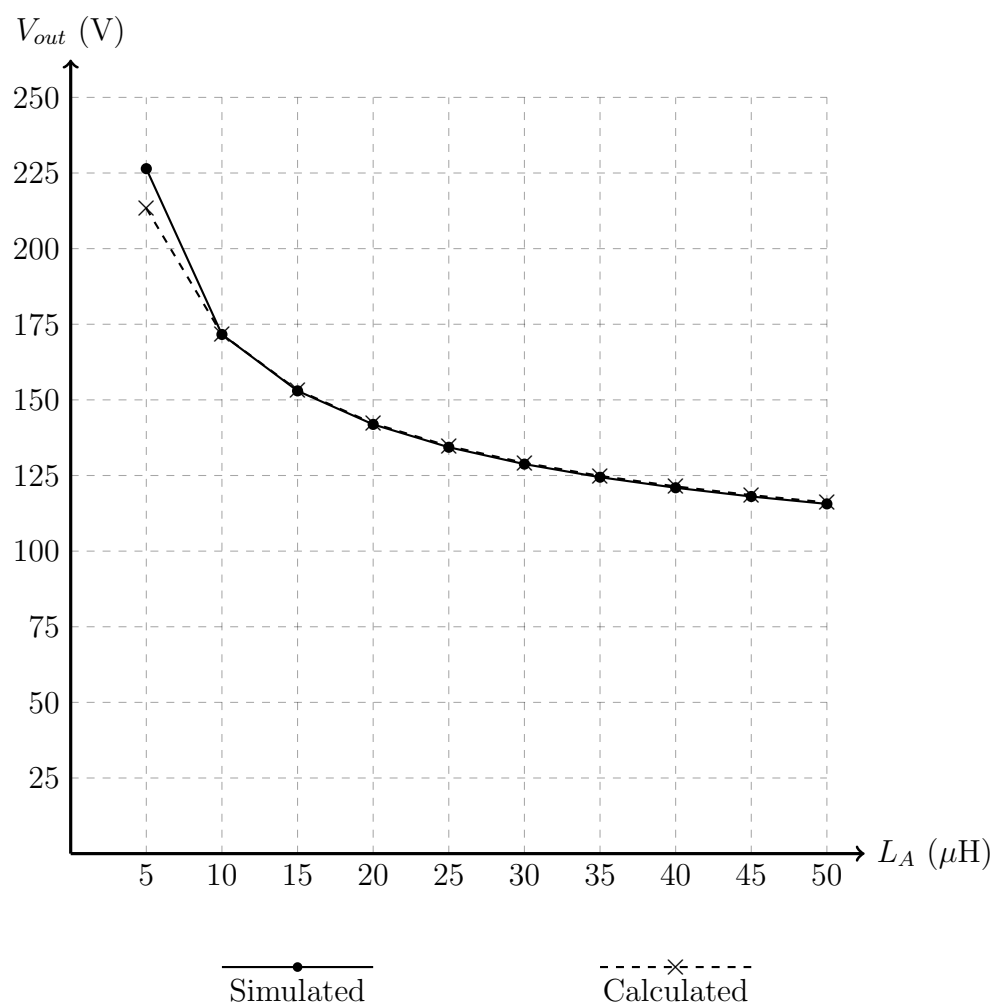


Fig. .15: Simulated vs calculated results for V_{out} while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$

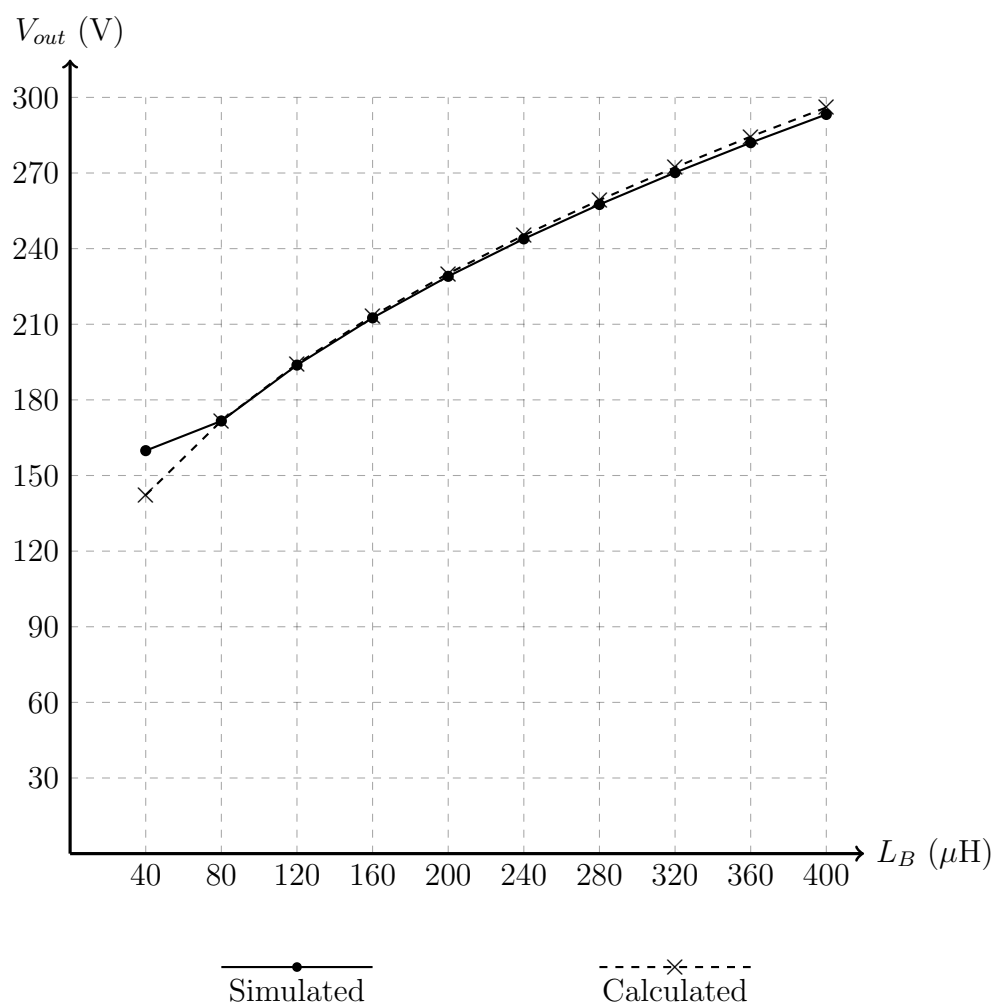


Fig. .16: Simulated vs calculated results for V_{out} while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$

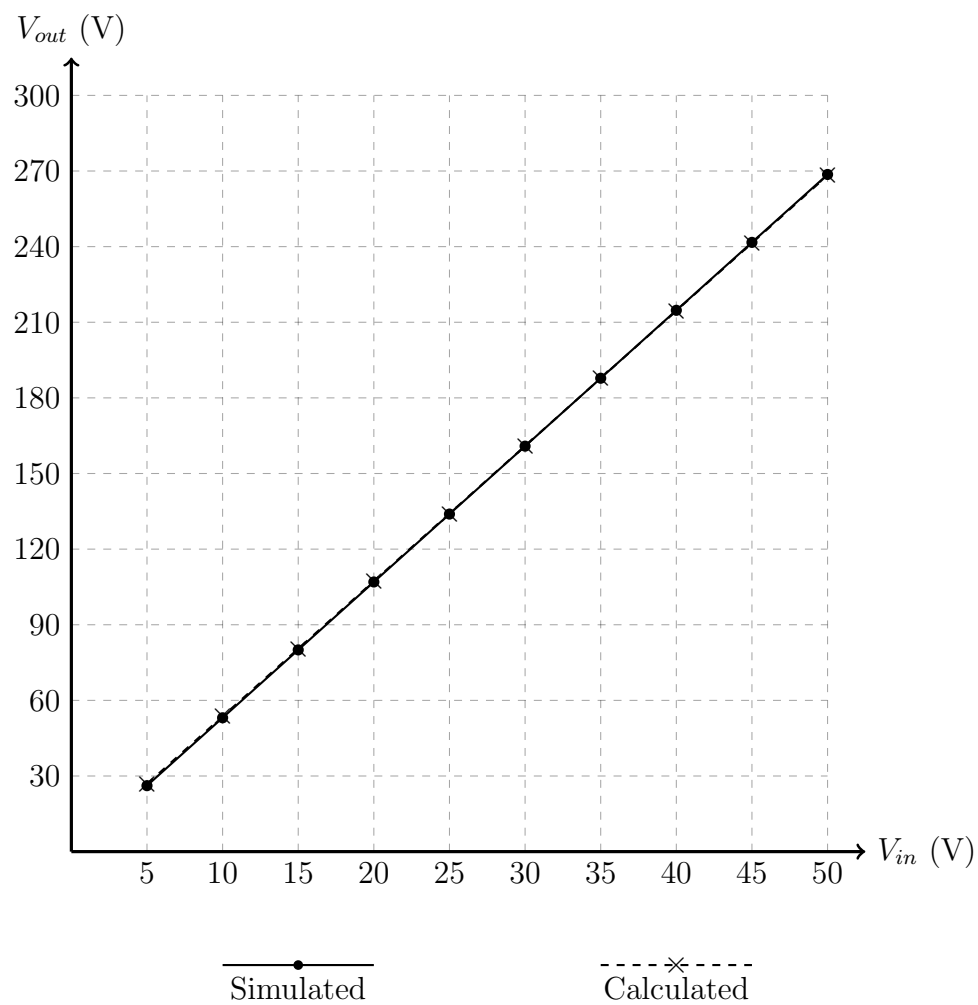


Fig. .17: Simulated vs calculated results for V_{out} while sweeping parameter V_{in} from 5V to 50V

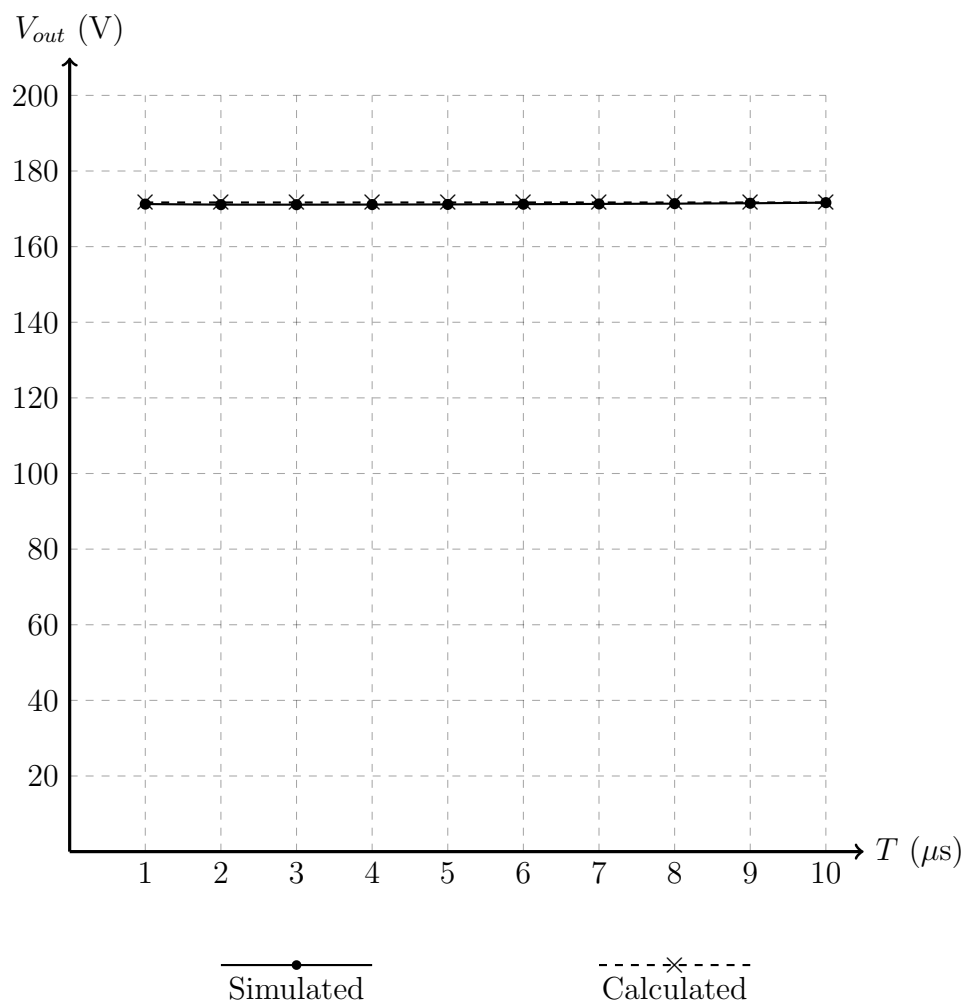


Fig. .18: Simulated vs calculated results for V_{out} while sweeping parameter T from $1\mu s$ to $10\mu s$

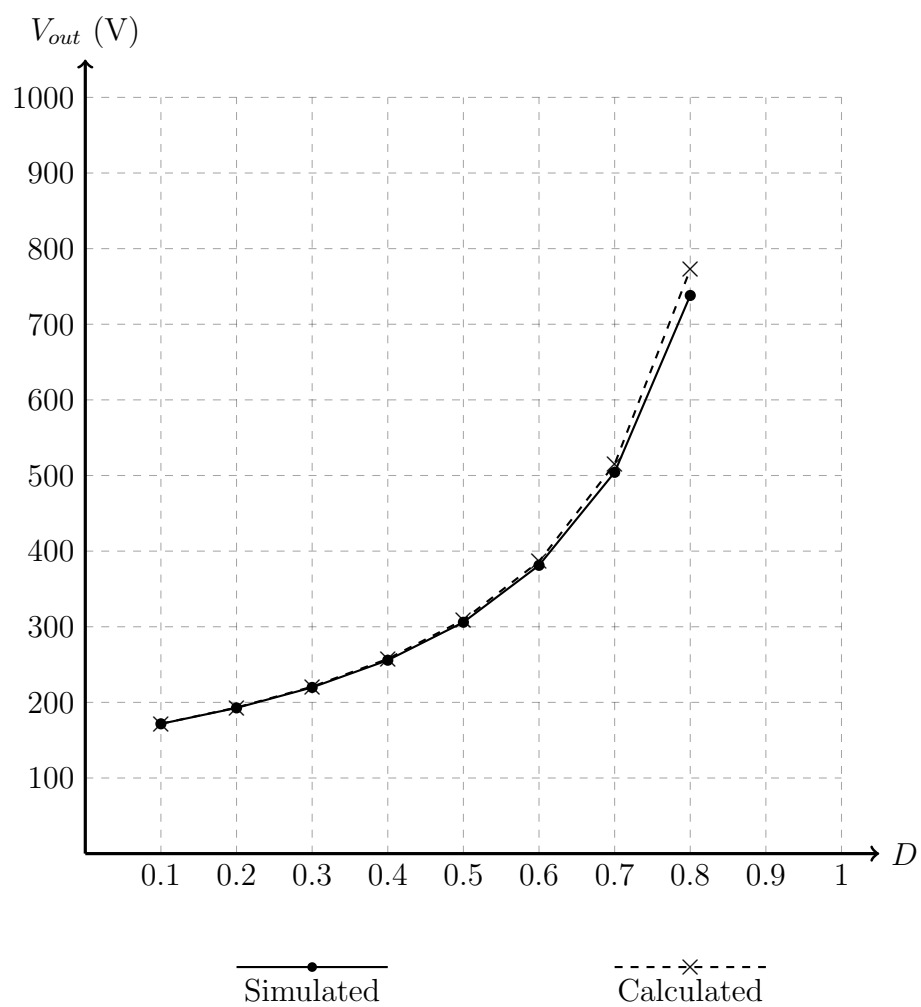


Fig. .19: Simulated vs calculated results for V_{out} while sweeping parameter D from 0.1 to 0.9

.7 Simulations for Constant Output Voltage Operation

In this section the significant equations derived in Section 2.0.3 are compared against simulation data. The following base parameters are used

$$L_{in} = 100\mu H$$

$$L_A = 10\mu H$$

$$L_B = 80\mu H$$

$$V_{in} = 32V$$

$$V_{out} = 400V$$

$$T = 10\mu s$$

$$D = 0.1$$

which closely emulates the application of boosting LV renewable sources into the UK mains power grid. In the following plots the circuit parameters maintain these values while a single parameter is swept across a range and all significant circuit variables are measured in each case.

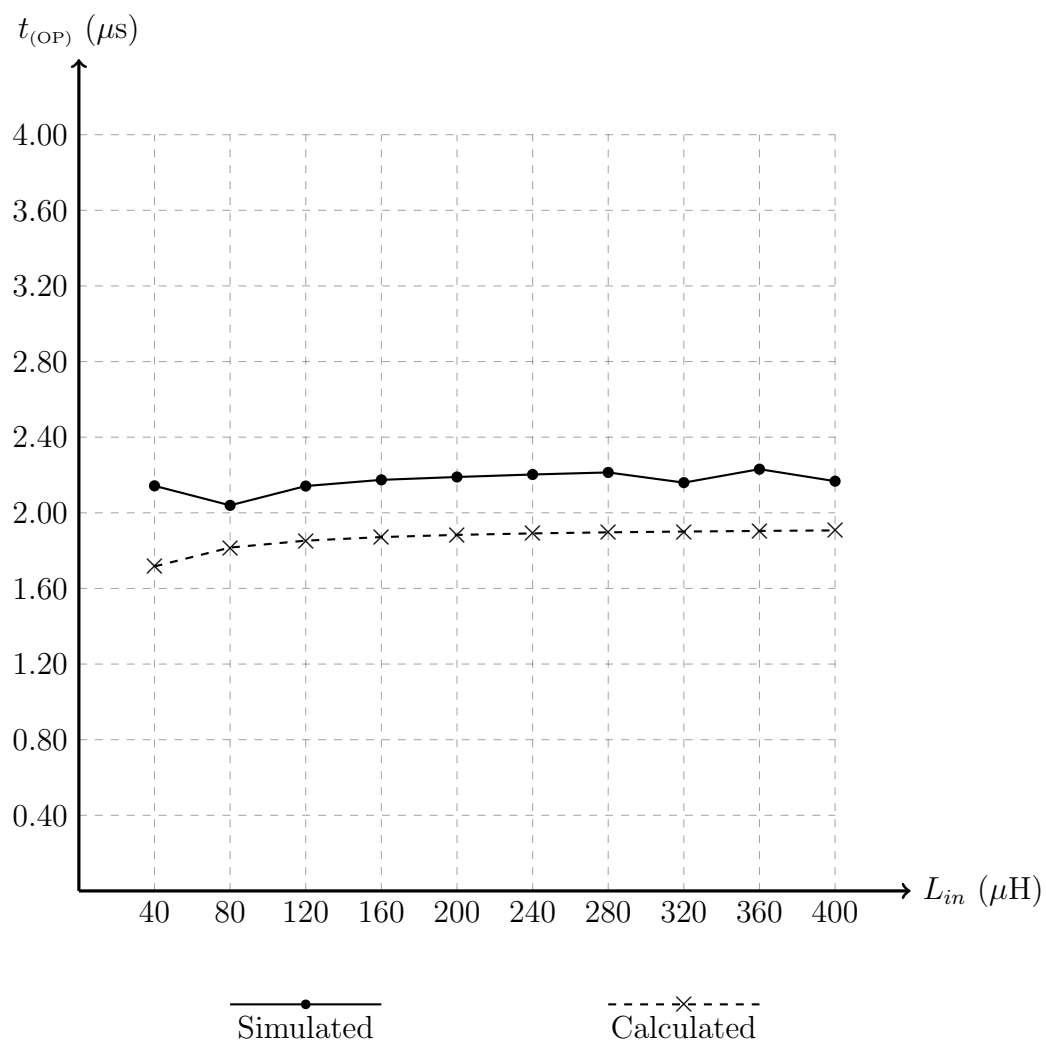


Fig. .20: Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter L_{in} from 40 μH to 400 μH

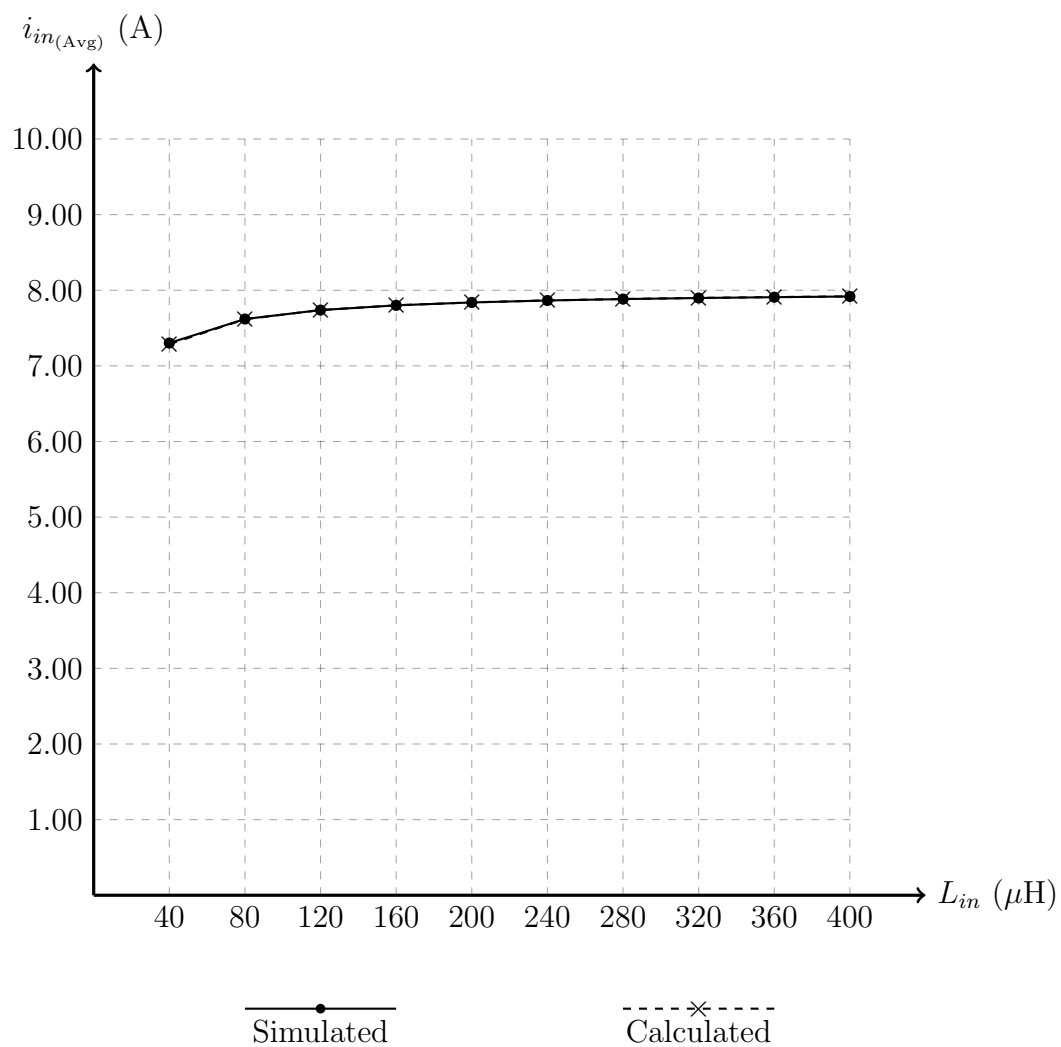


Fig. .21: Simulated vs calculated results for $i_{in(\text{Avg})}$ while sweeping parameter L_{in} from $40\mu\text{H}$ to $400\mu\text{H}$

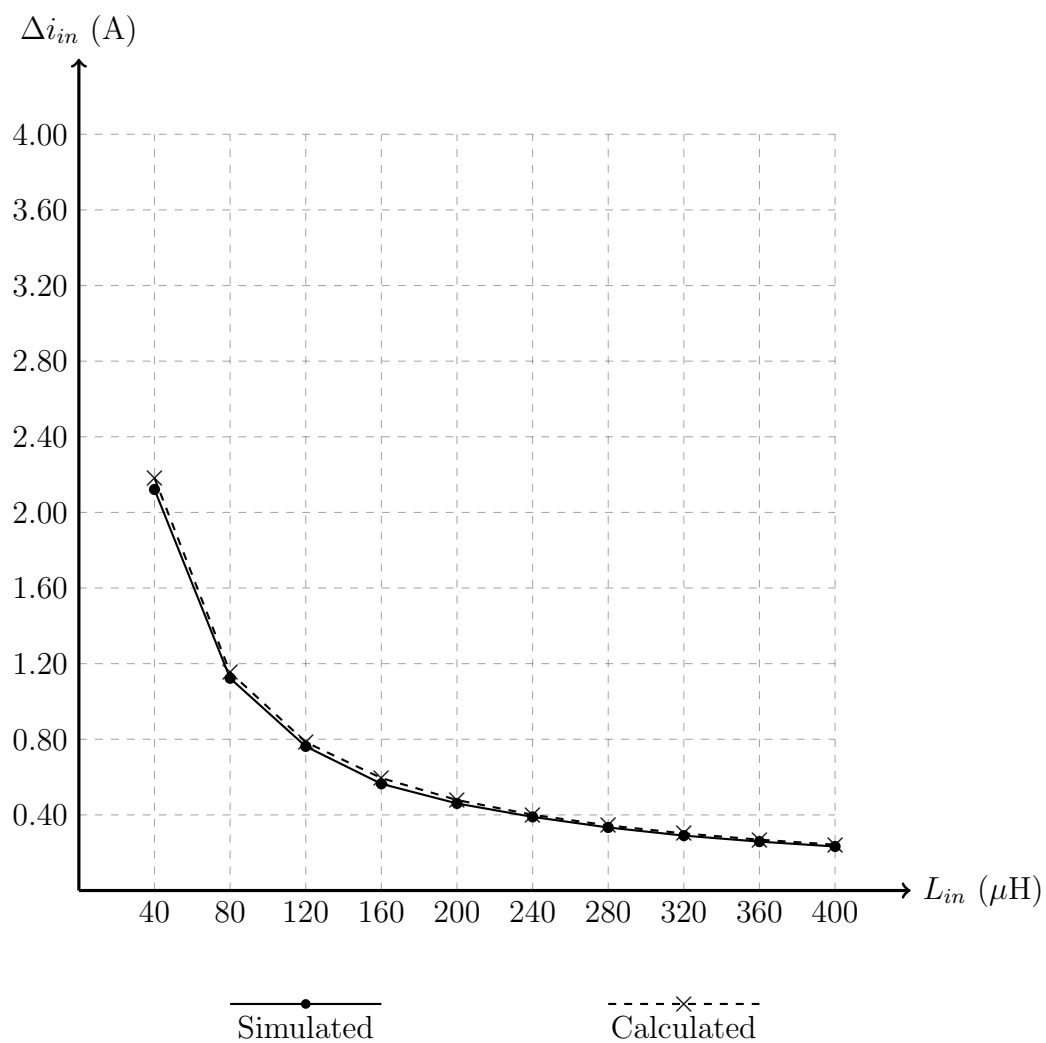


Fig. .22: Simulated vs calculated results for Δi_{in} while sweeping parameter L_{in} from $40\mu\text{H}$ to $400\mu\text{H}$

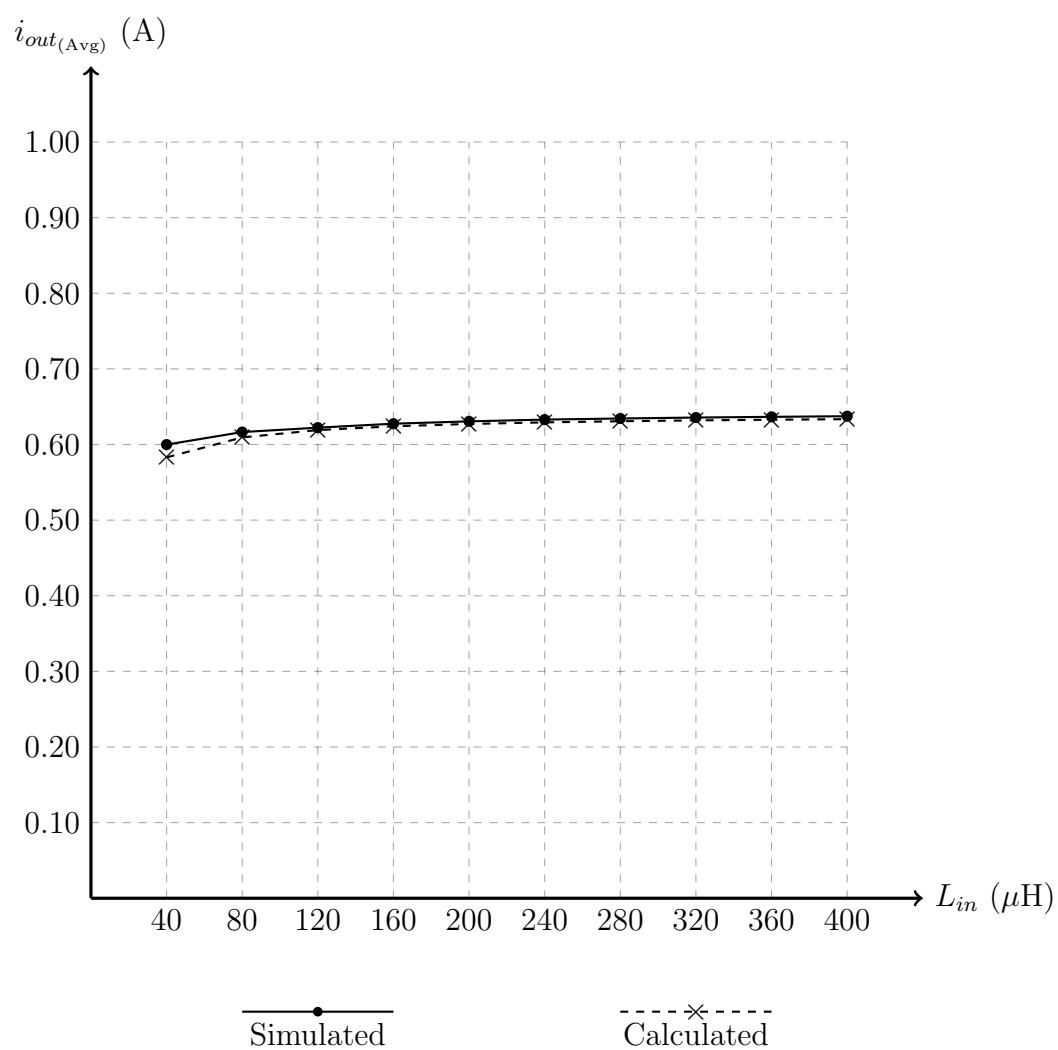


Fig. .23: Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter L_{in} from $40\mu H$ to $400\mu H$

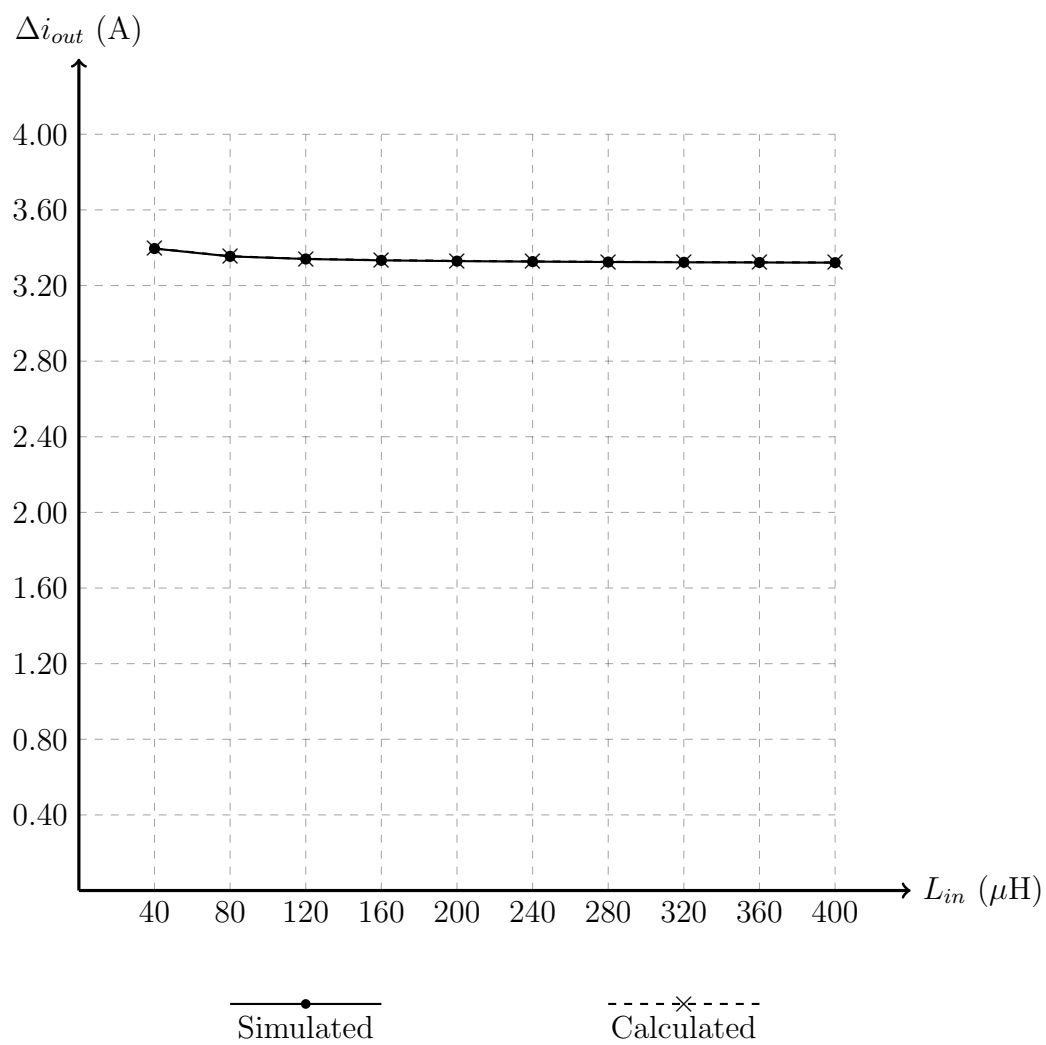


Fig. .24: Simulated vs calculated results for Δi_{out} while sweeping parameter L_{in} from $40\mu\text{H}$ to $400\mu\text{H}$

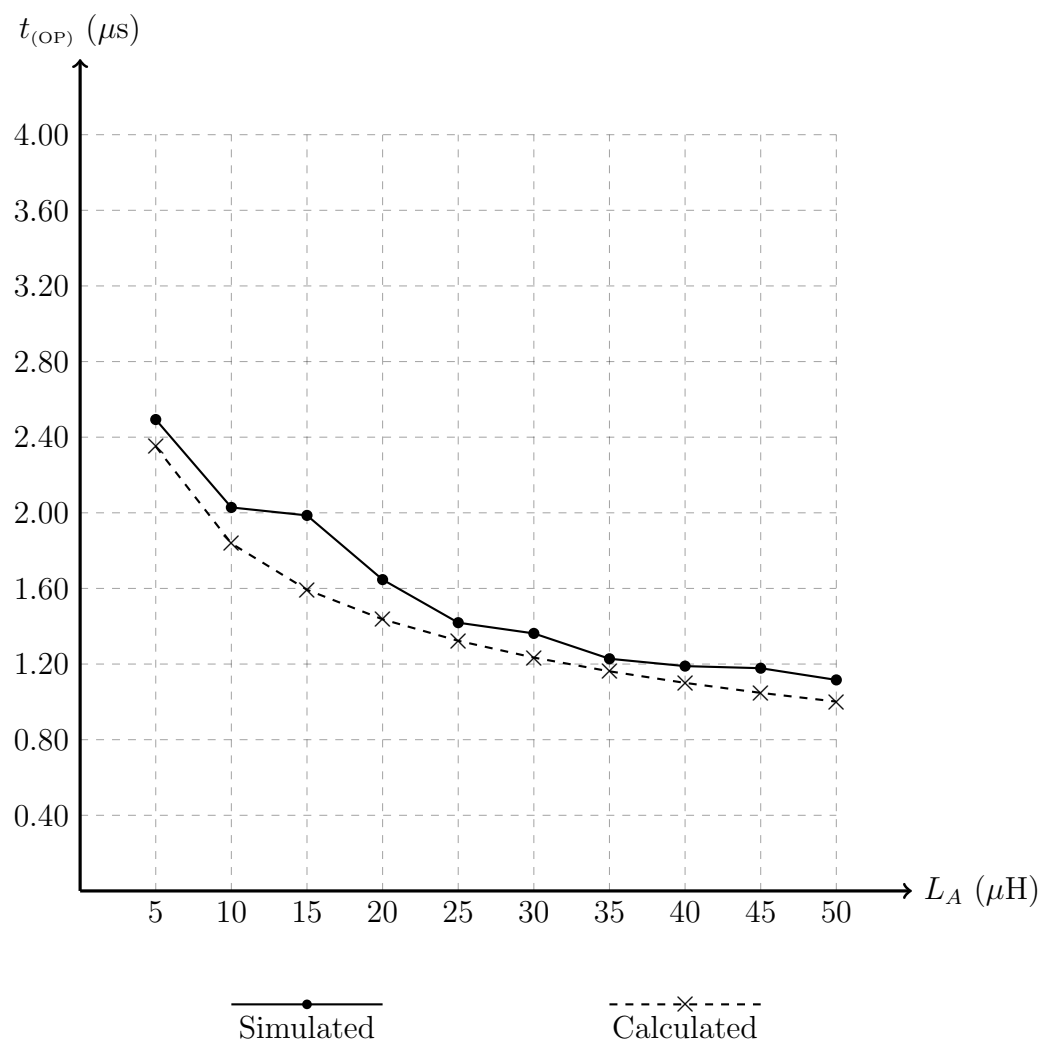


Fig. .25: Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$

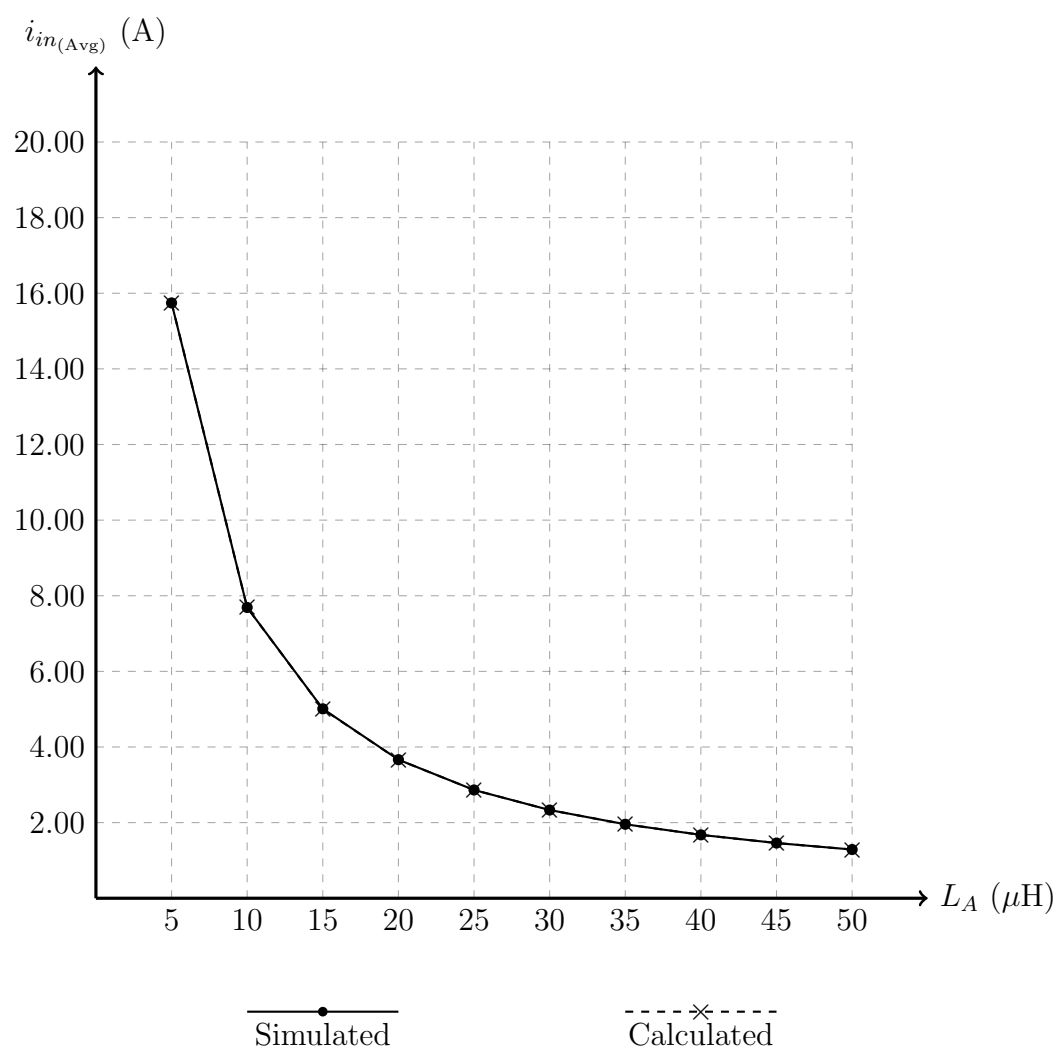


Fig. .26: Simulated vs calculated results for $i_{in(\text{Avg})}$ while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$

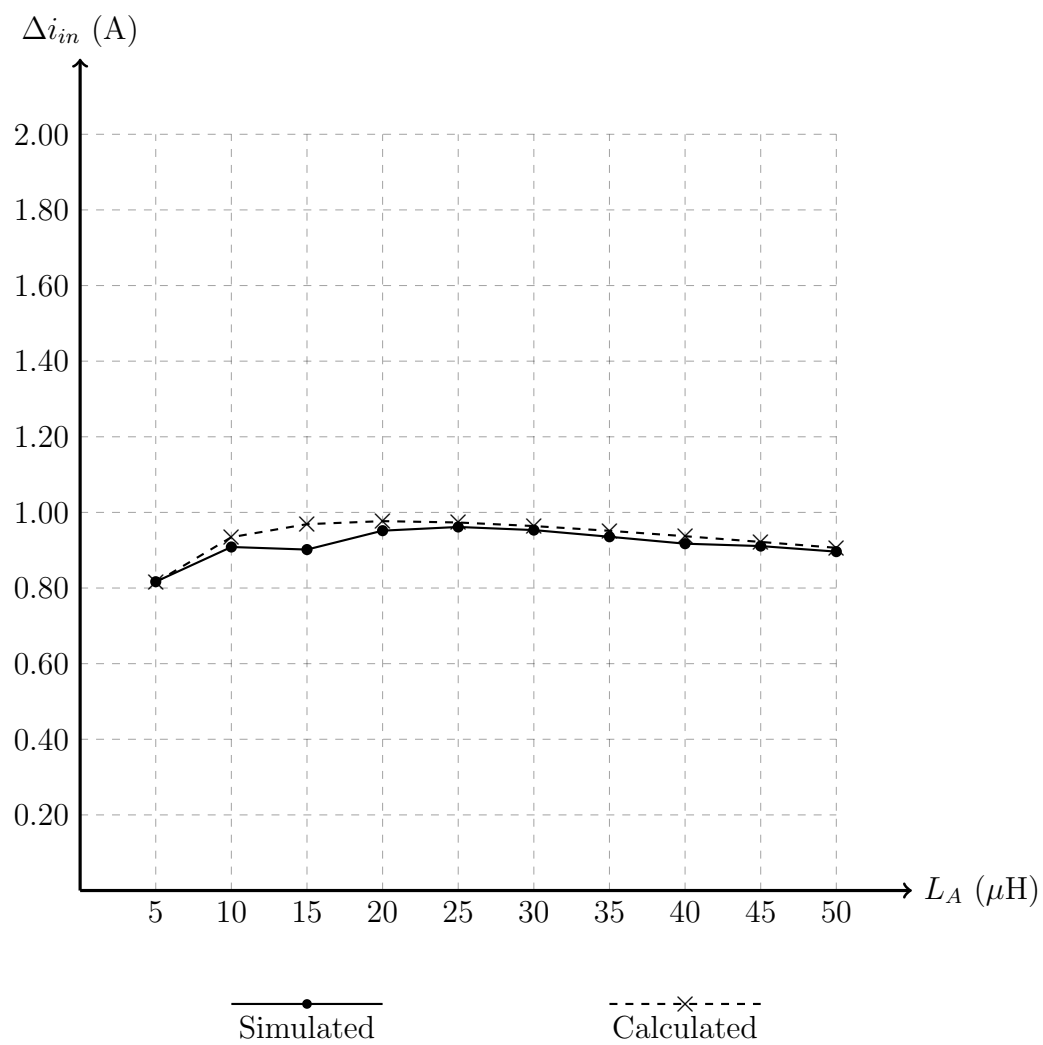


Fig. .27: Simulated vs calculated results for Δi_{in} while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$

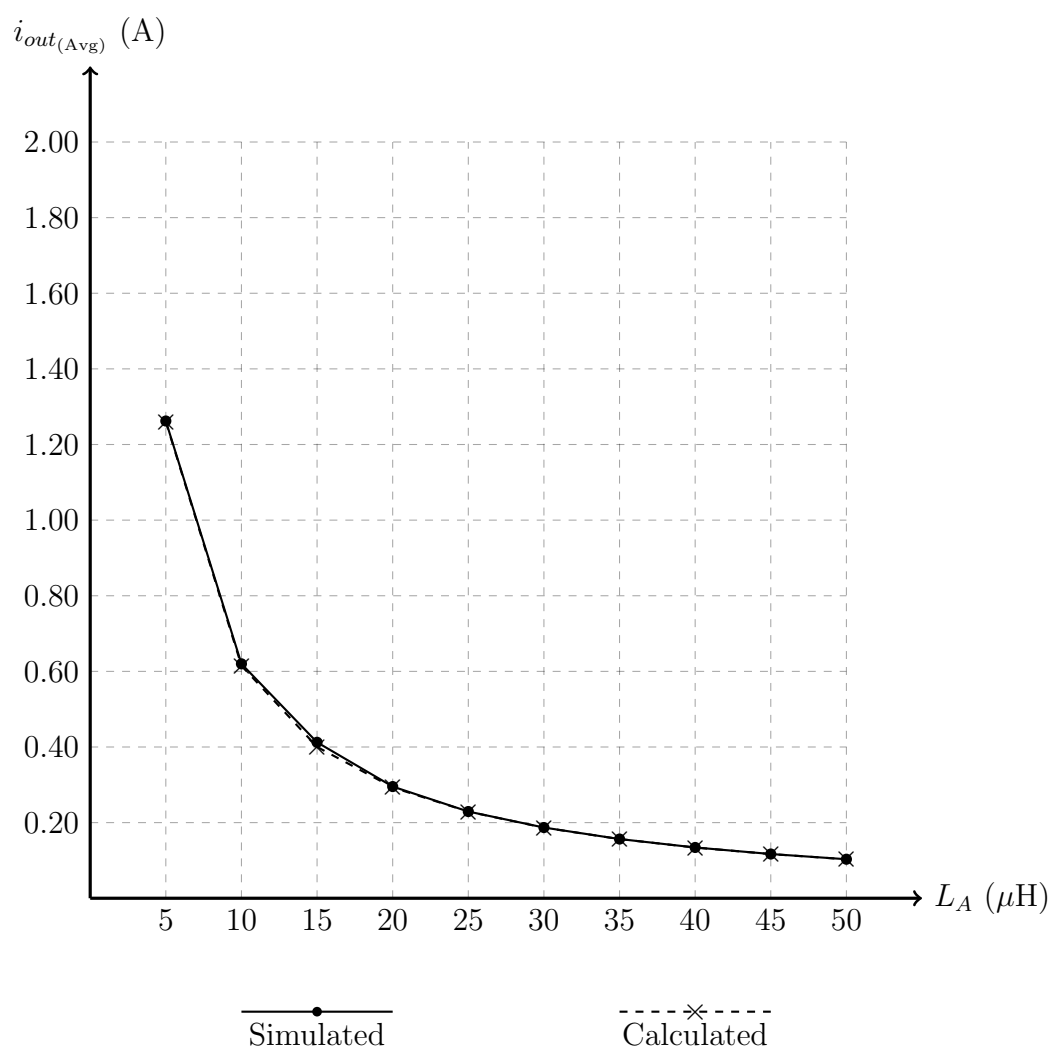


Fig. .28: Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$

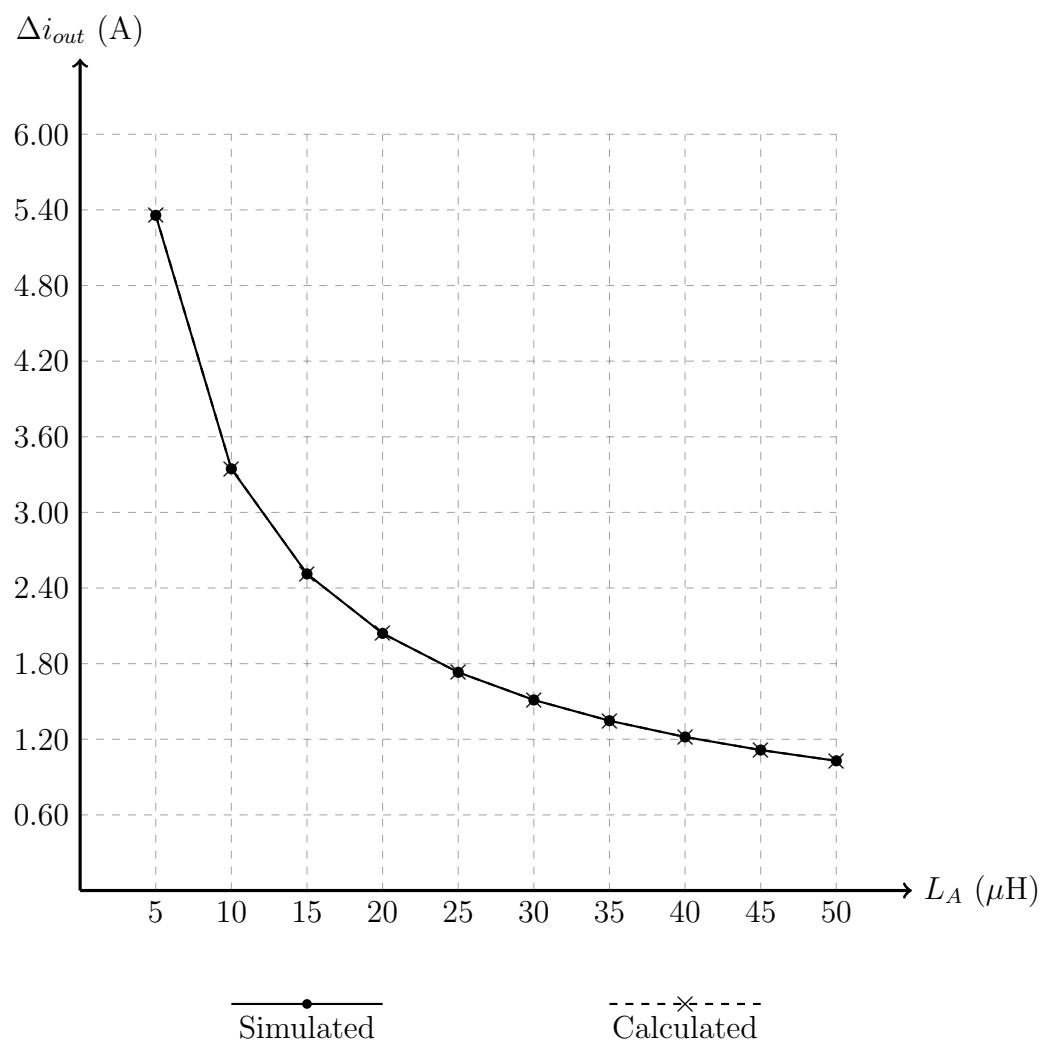


Fig. .29: Simulated vs calculated results for Δi_{out} while sweeping parameter L_A from $5\mu\text{H}$ to $50\mu\text{H}$

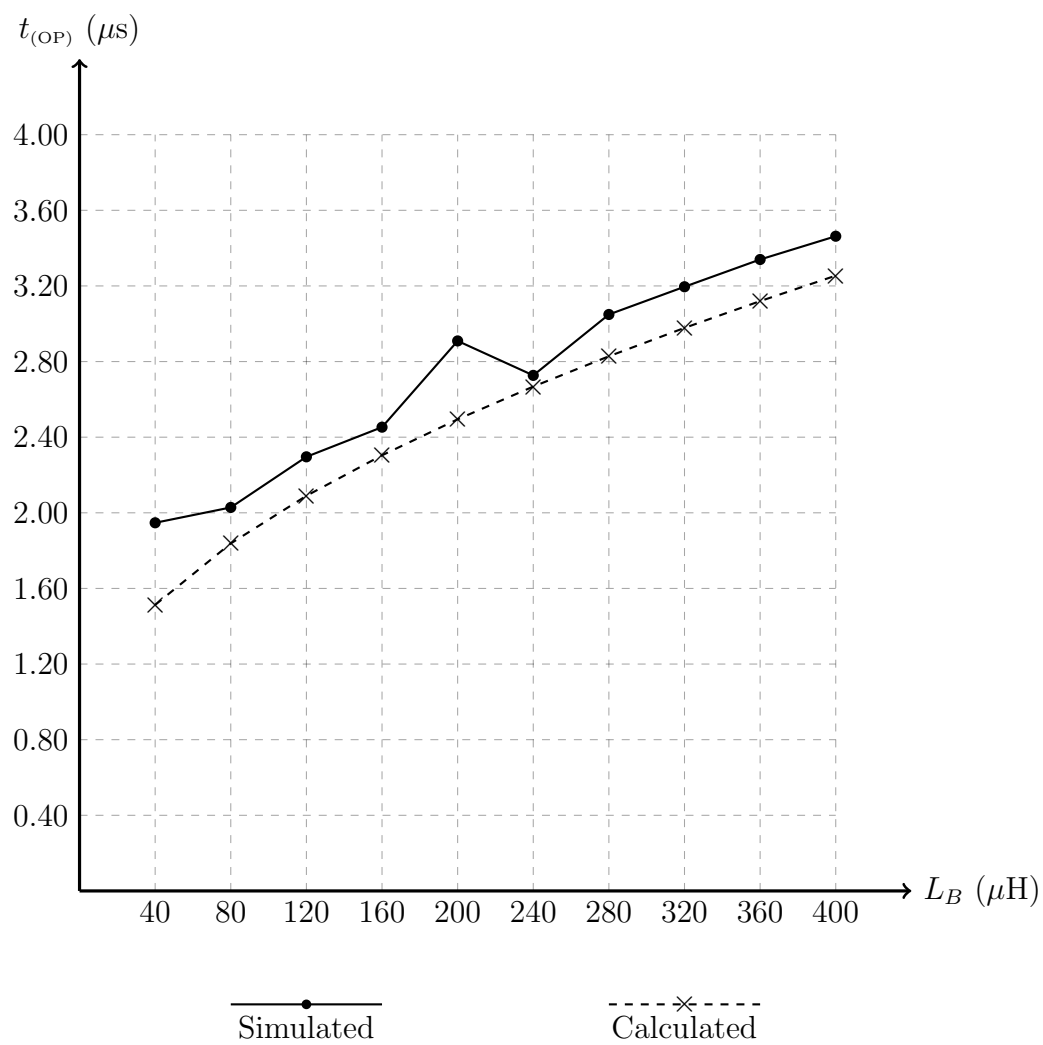


Fig. .30: Simulated vs calculated results for $t_{(\text{OP})}$ while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$

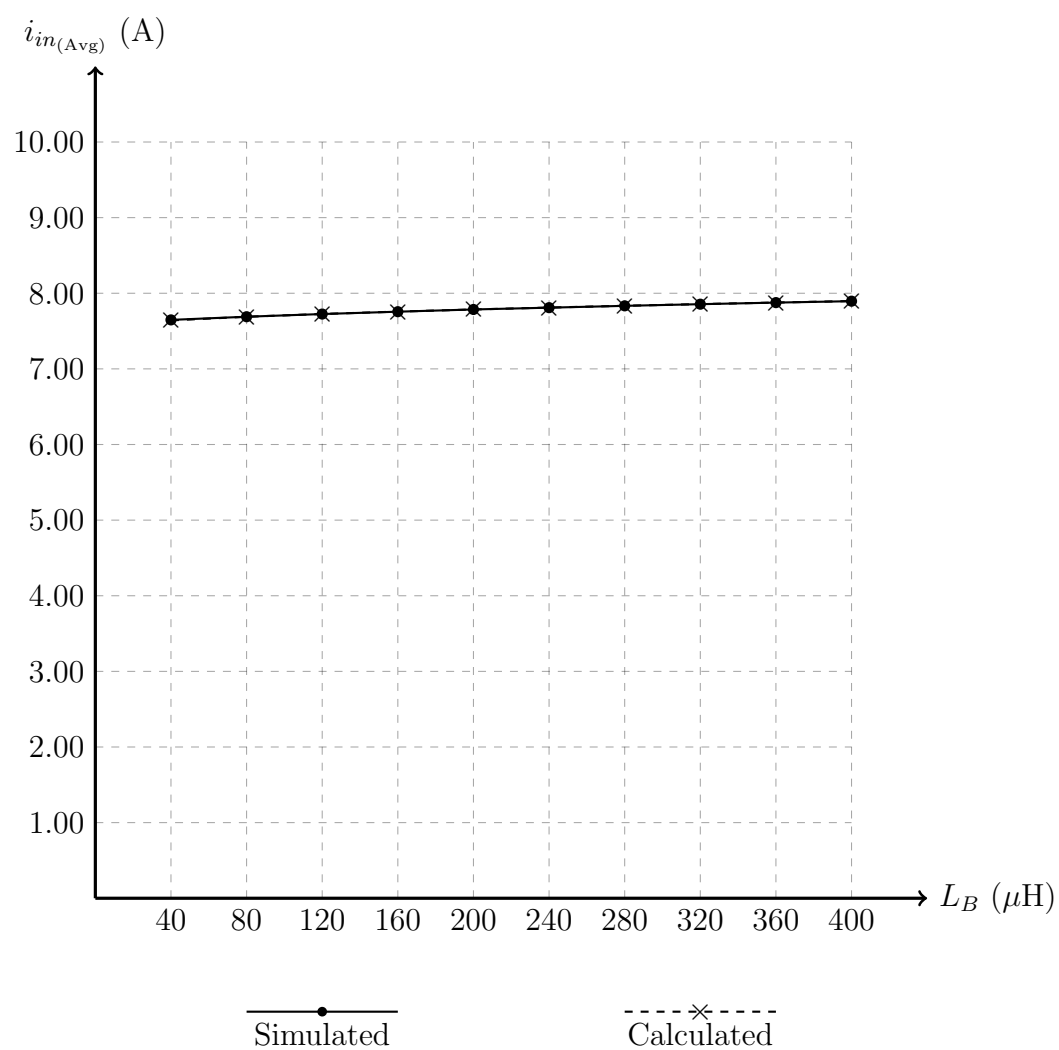


Fig. .31: Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter L_B from $40\mu H$ to $400\mu H$

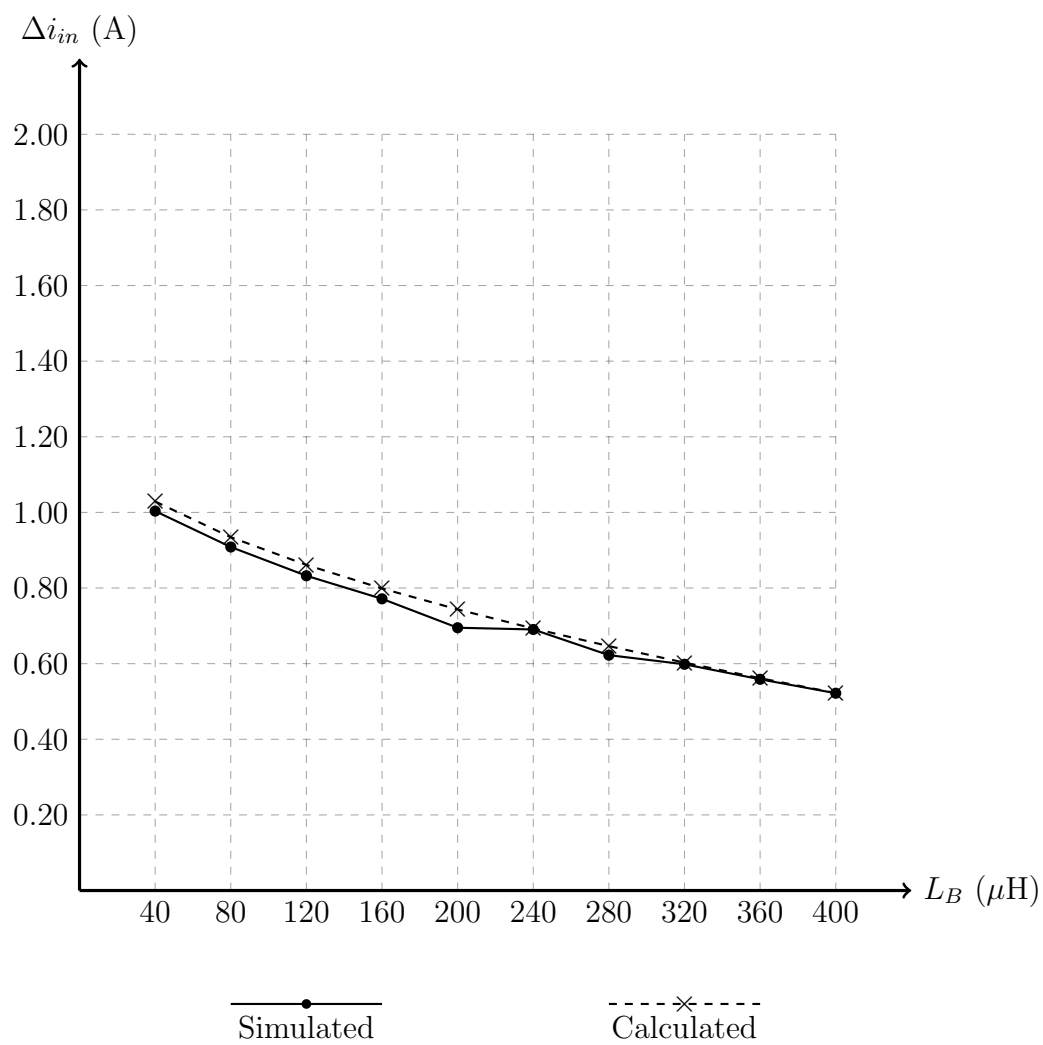


Fig. .32: Simulated vs calculated results for Δi_{in} while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$

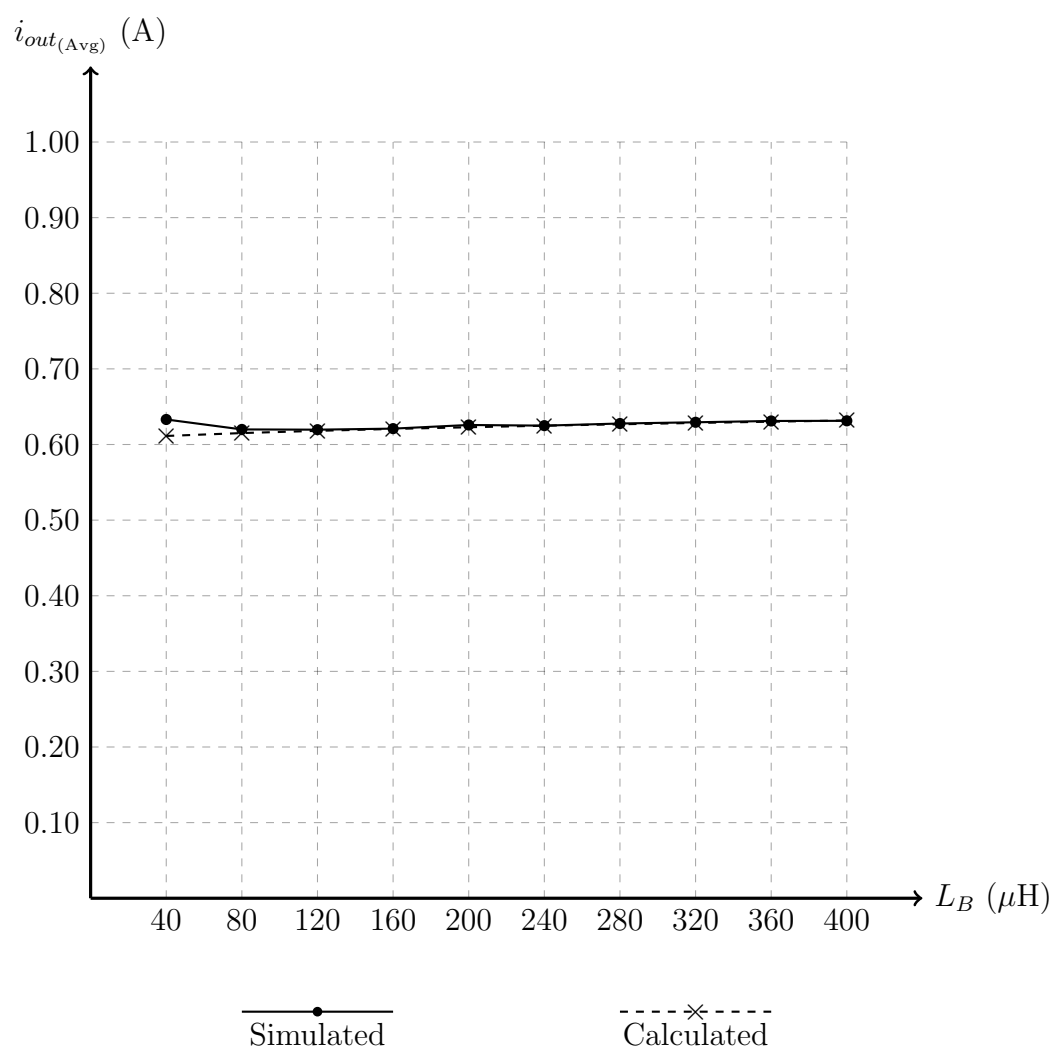


Fig. .33: Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$

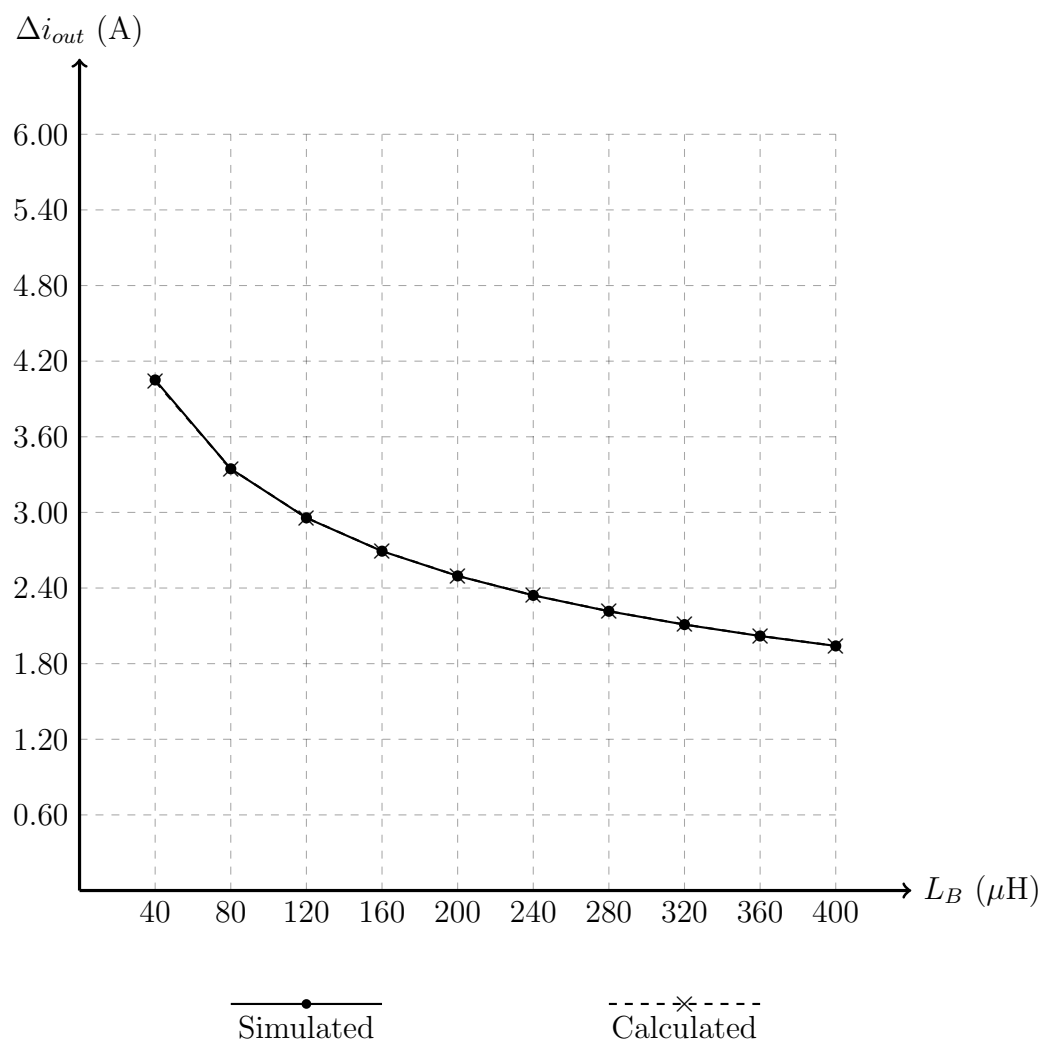


Fig. .34: Simulated vs calculated results for Δi_{out} while sweeping parameter L_B from $40\mu\text{H}$ to $400\mu\text{H}$

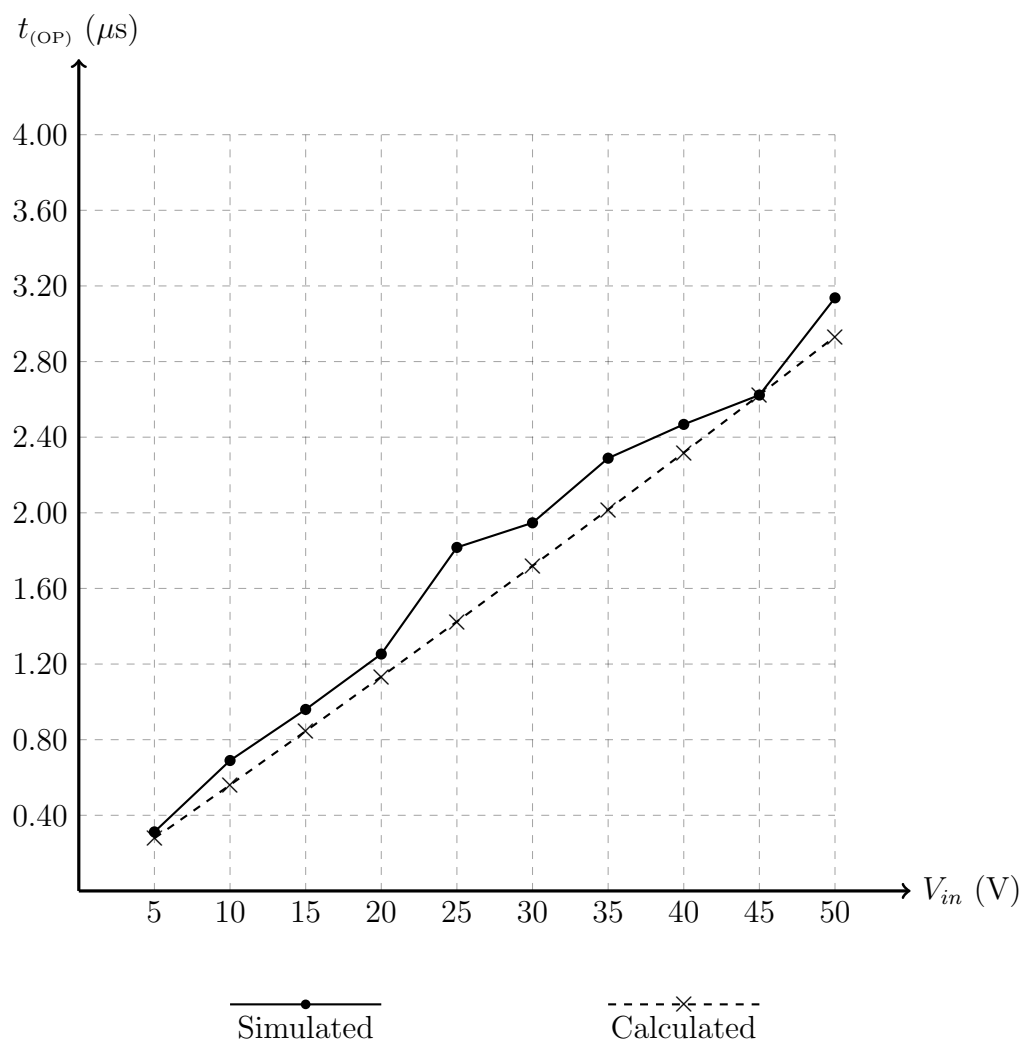


Fig. .35: Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter V_{in} from 5V to 50V

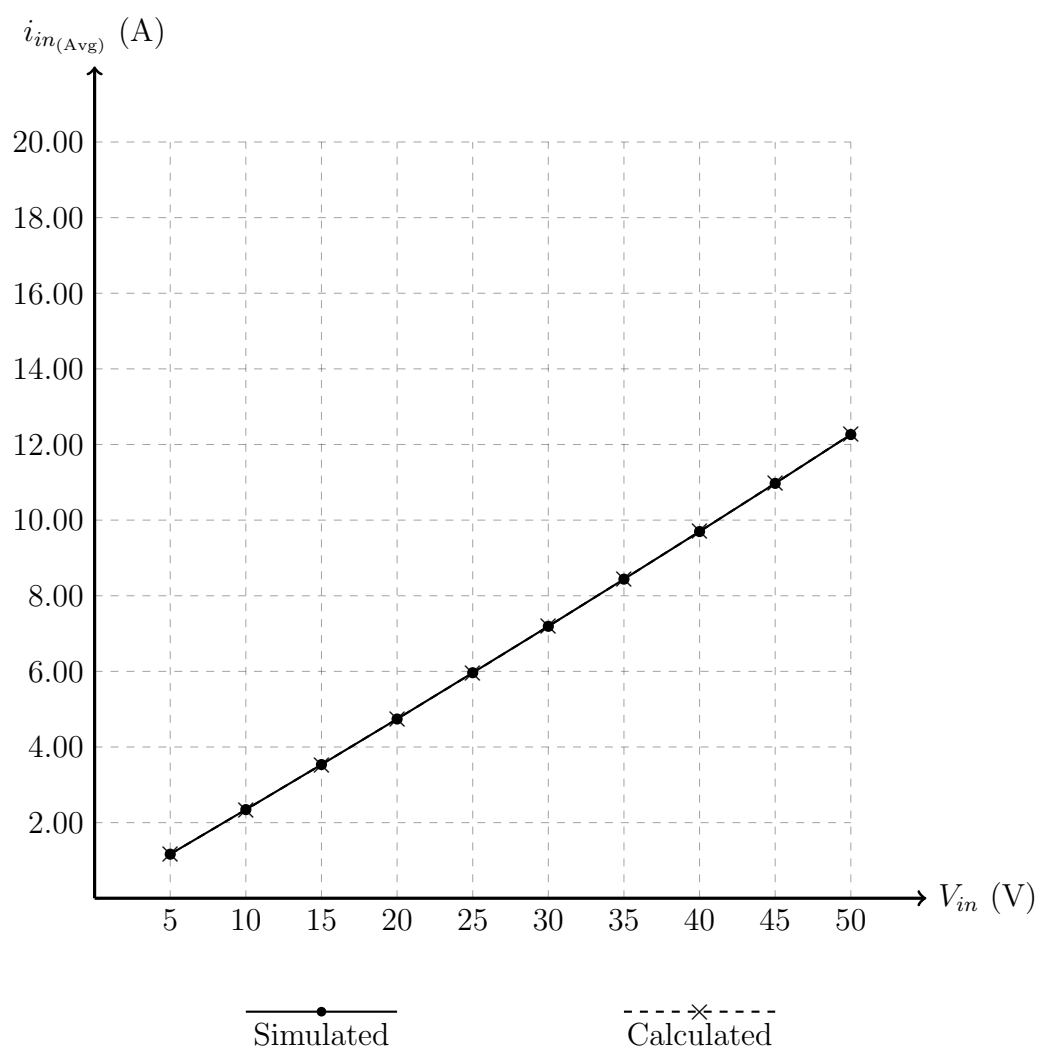


Fig. .36: Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter V_{in} from 5V to 50V

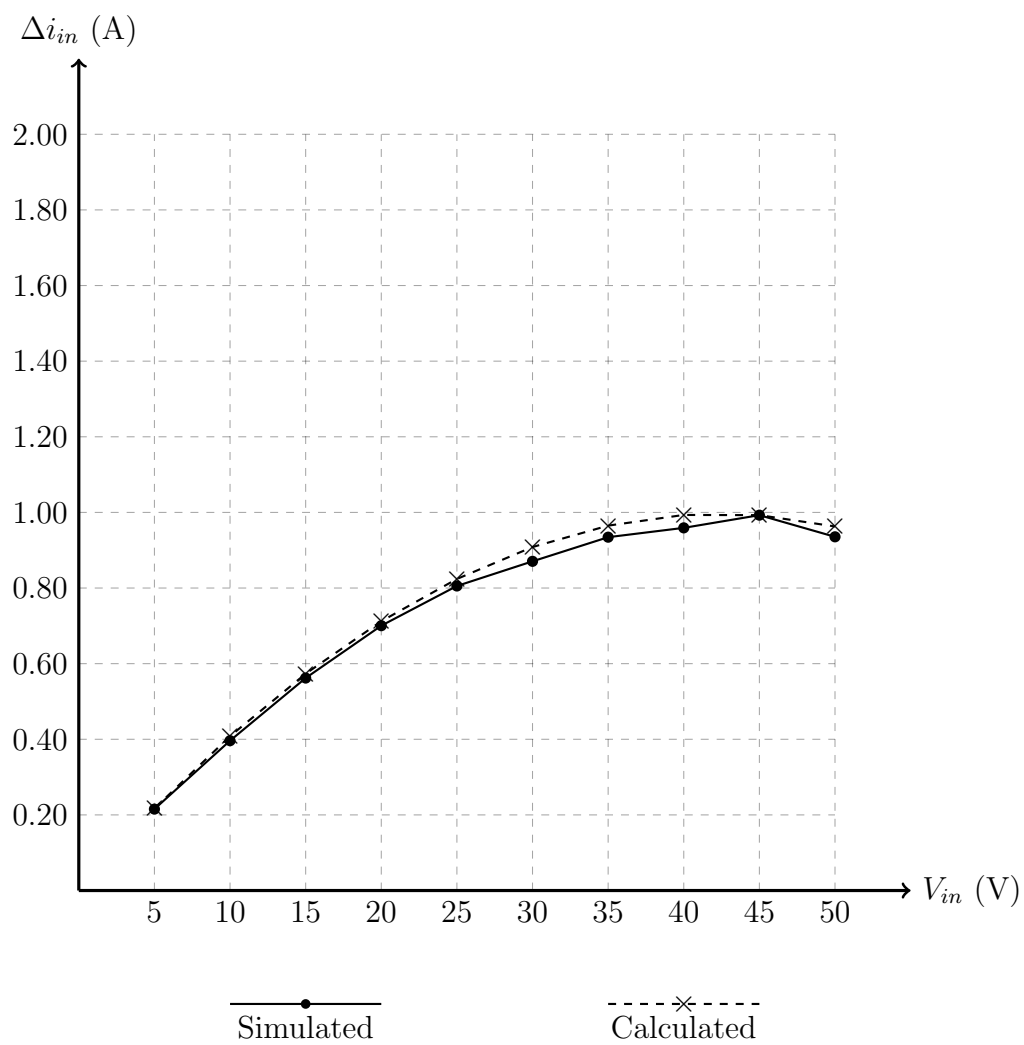


Fig. .37: Simulated vs calculated results for Δi_{in} while sweeping parameter V_{in} from 5V to 50V

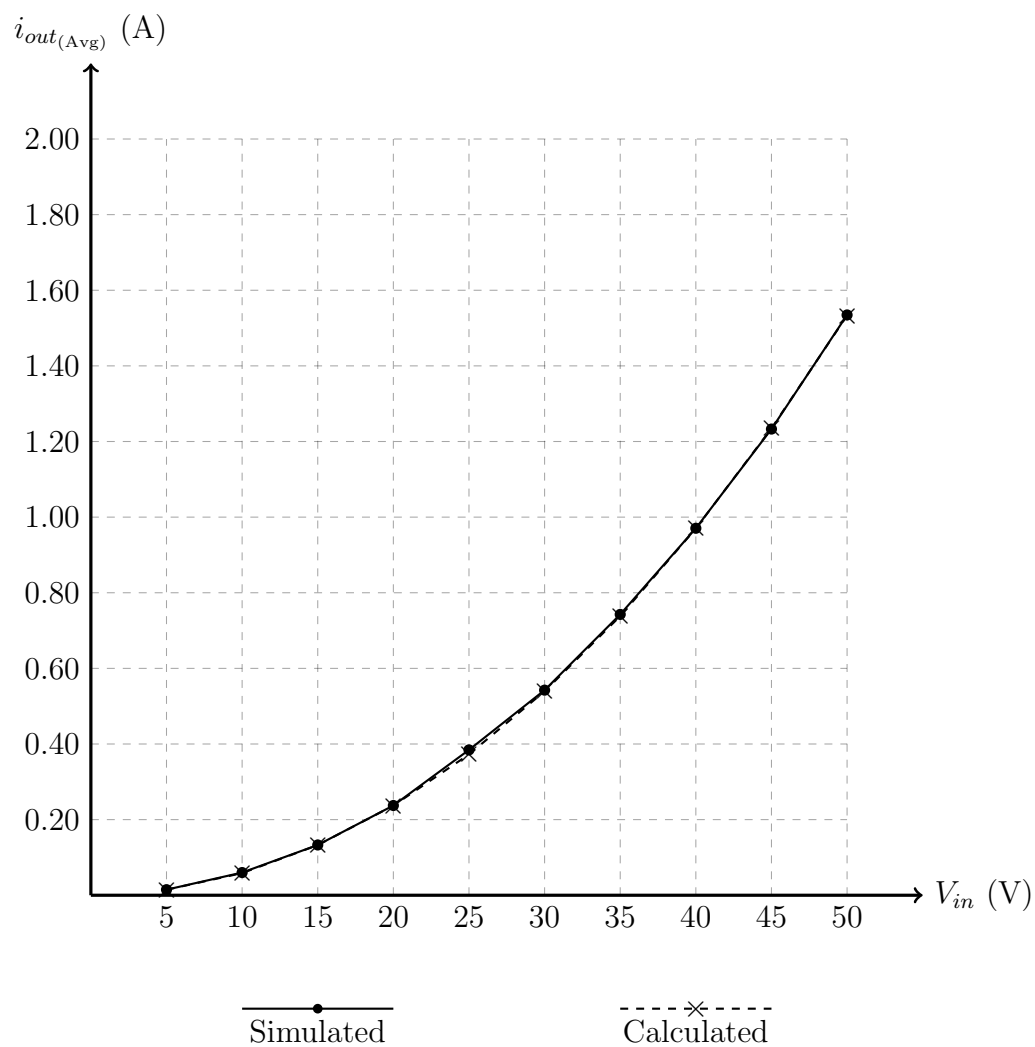


Fig. .38: Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter V_{in} from 5V to 50V

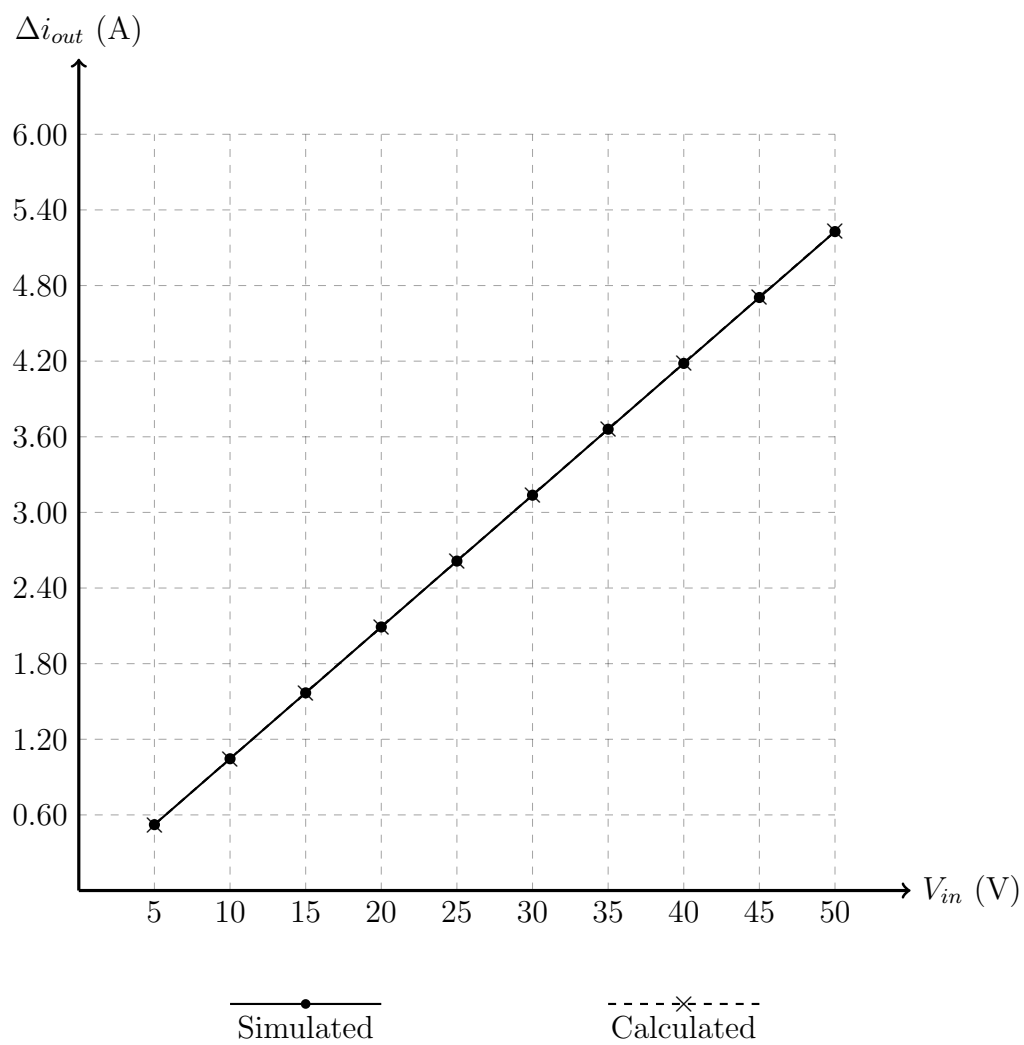


Fig. .39: Simulated vs calculated results for Δi_{out} while sweeping parameter V_{in} from 5V to 50V

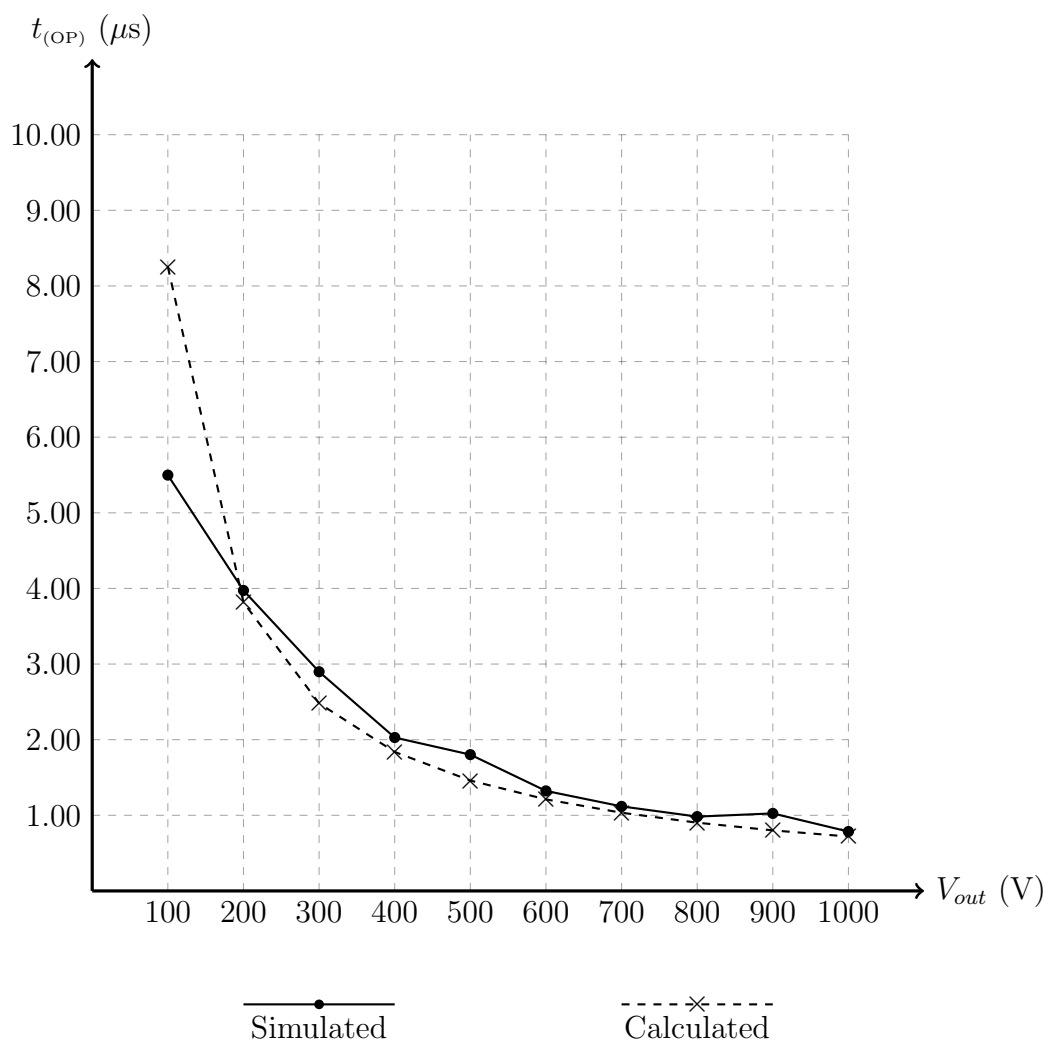


Fig. .40: Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter V_{out} from 100V to 1000V

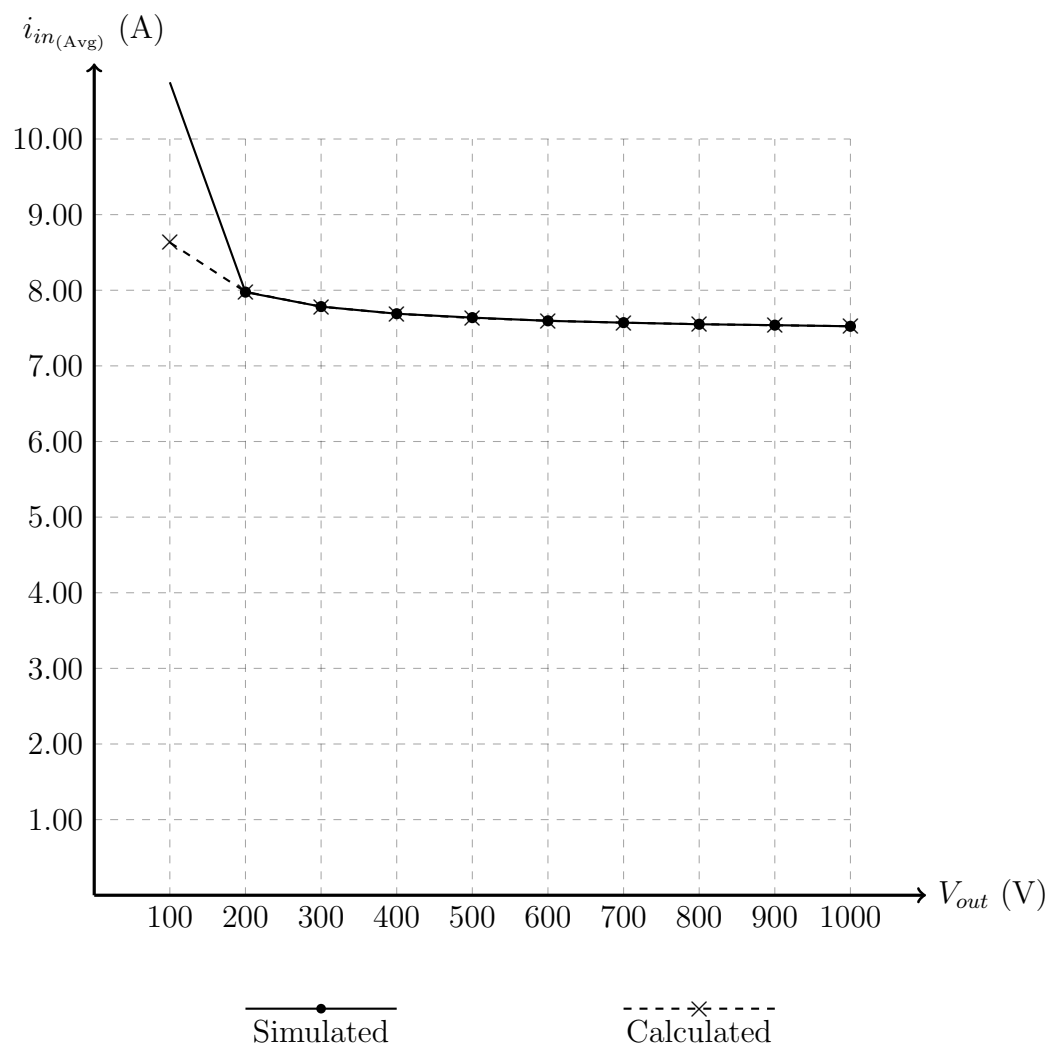


Fig. .41: Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter V_{out} from 100V to 1000V

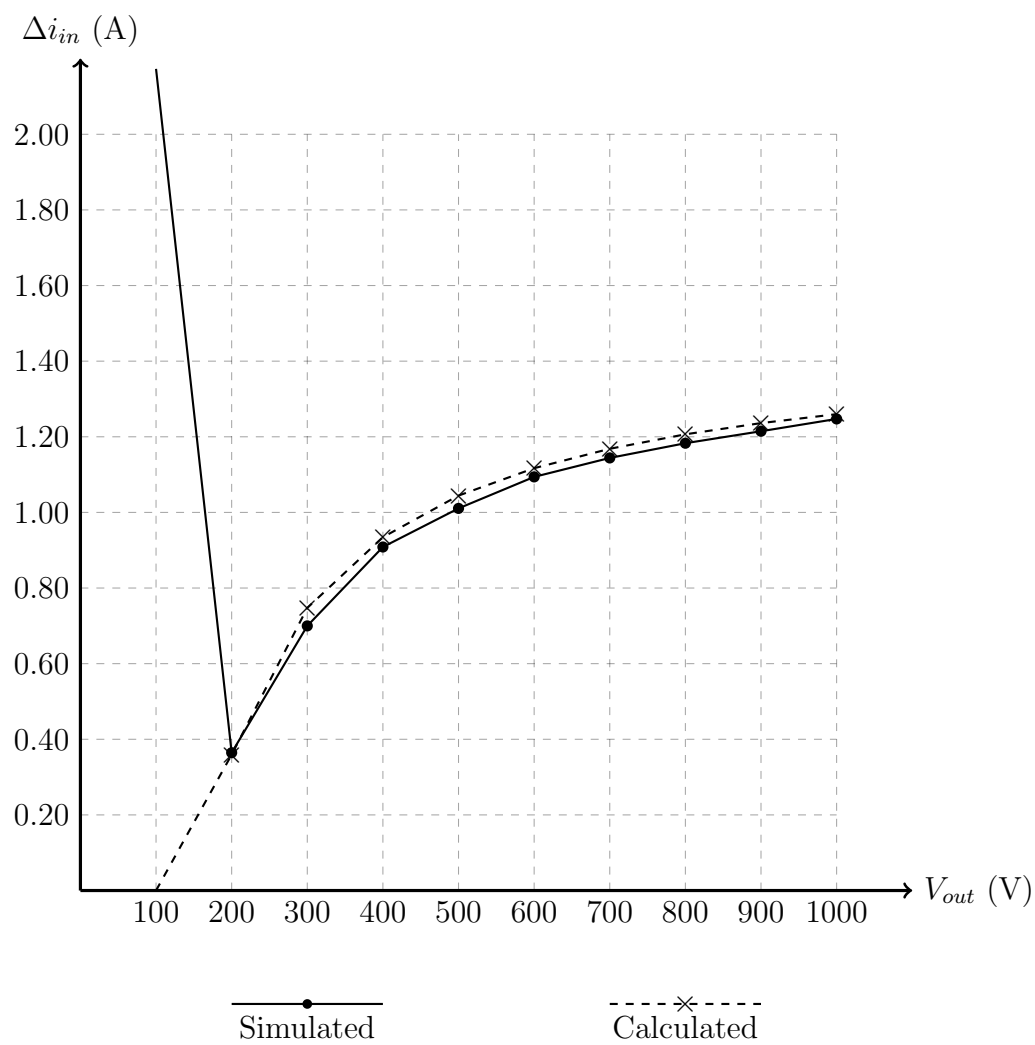


Fig. .42: Simulated vs calculated results for Δi_{in} while sweeping parameter V_{out} from 100V to 1000V

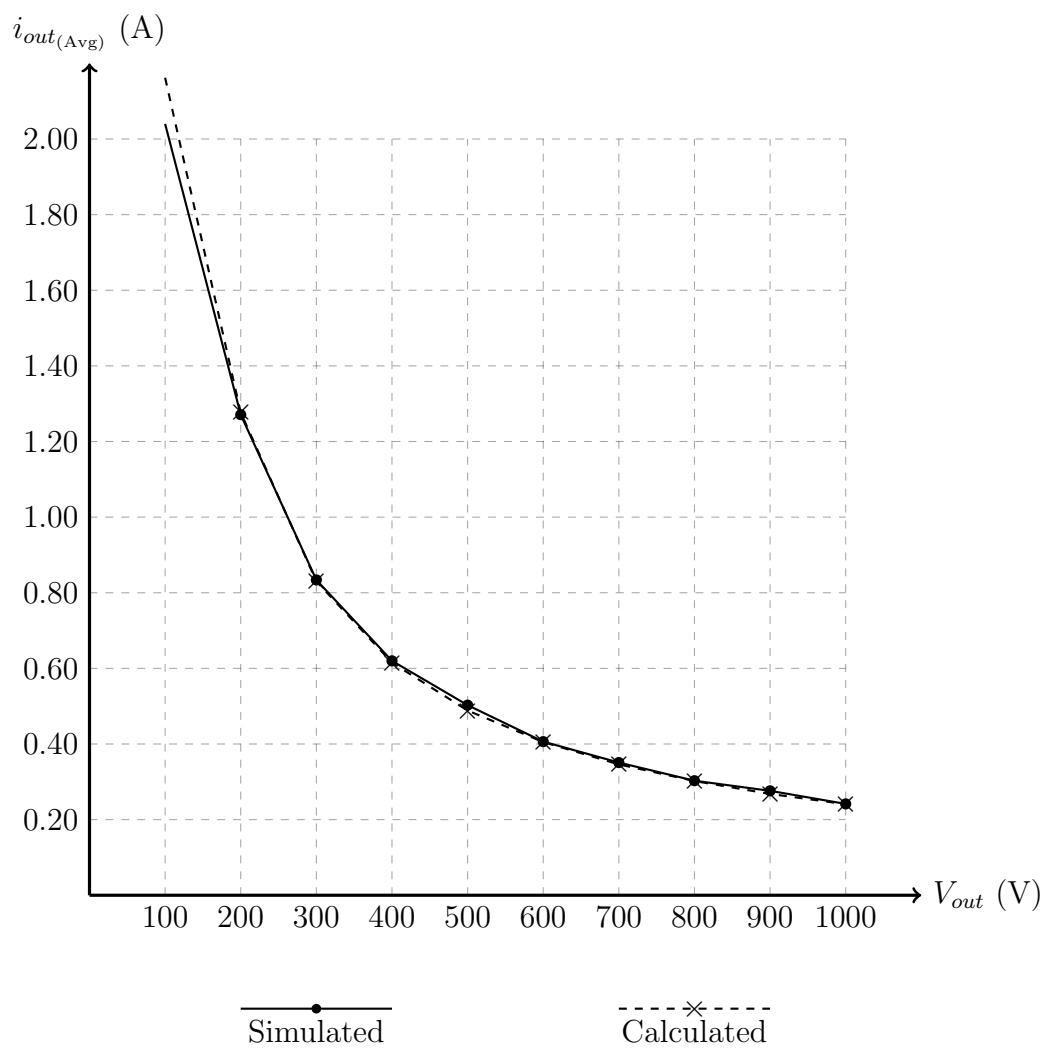


Fig. .43: Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter V_{out} from 100V to 1000V

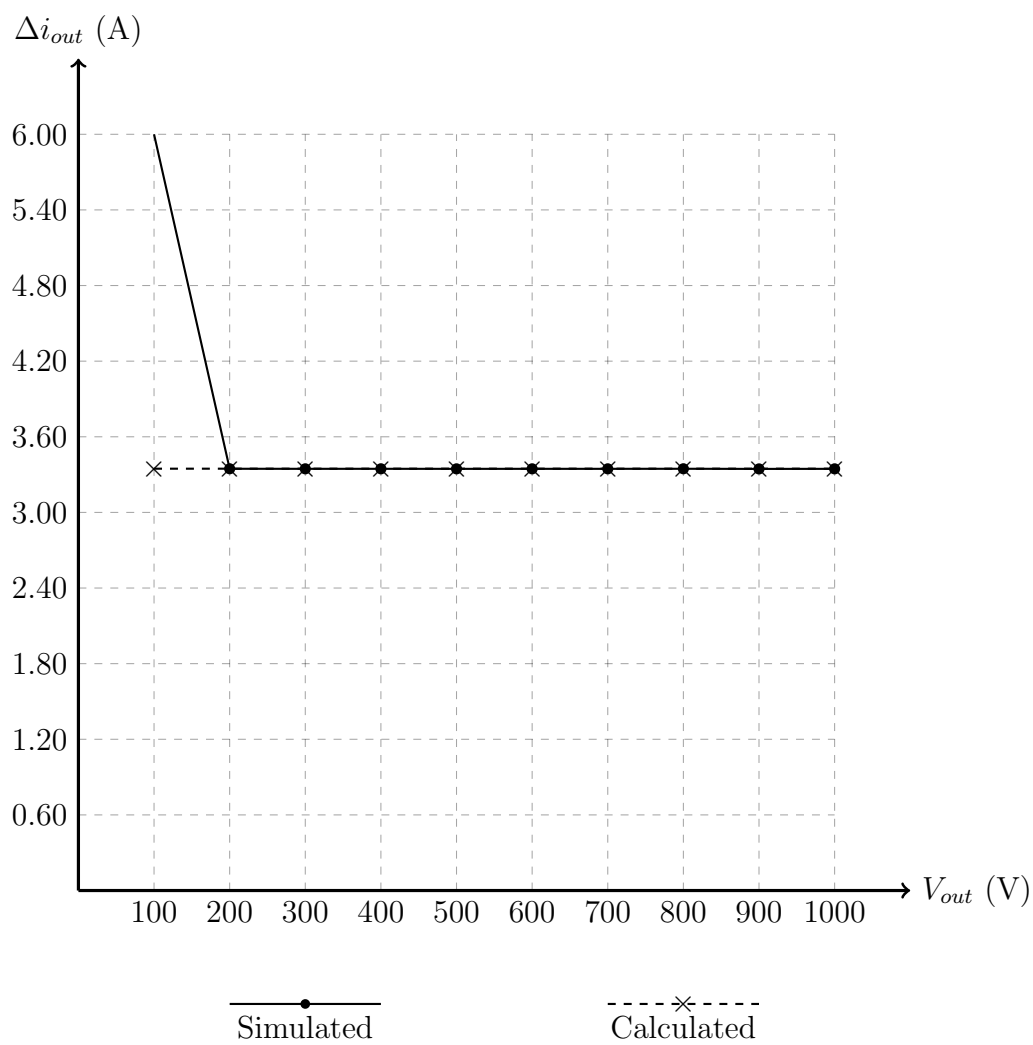


Fig. .44: Simulated vs calculated results for Δi_{out} while sweeping parameter V_{out} from 100V to 1000V

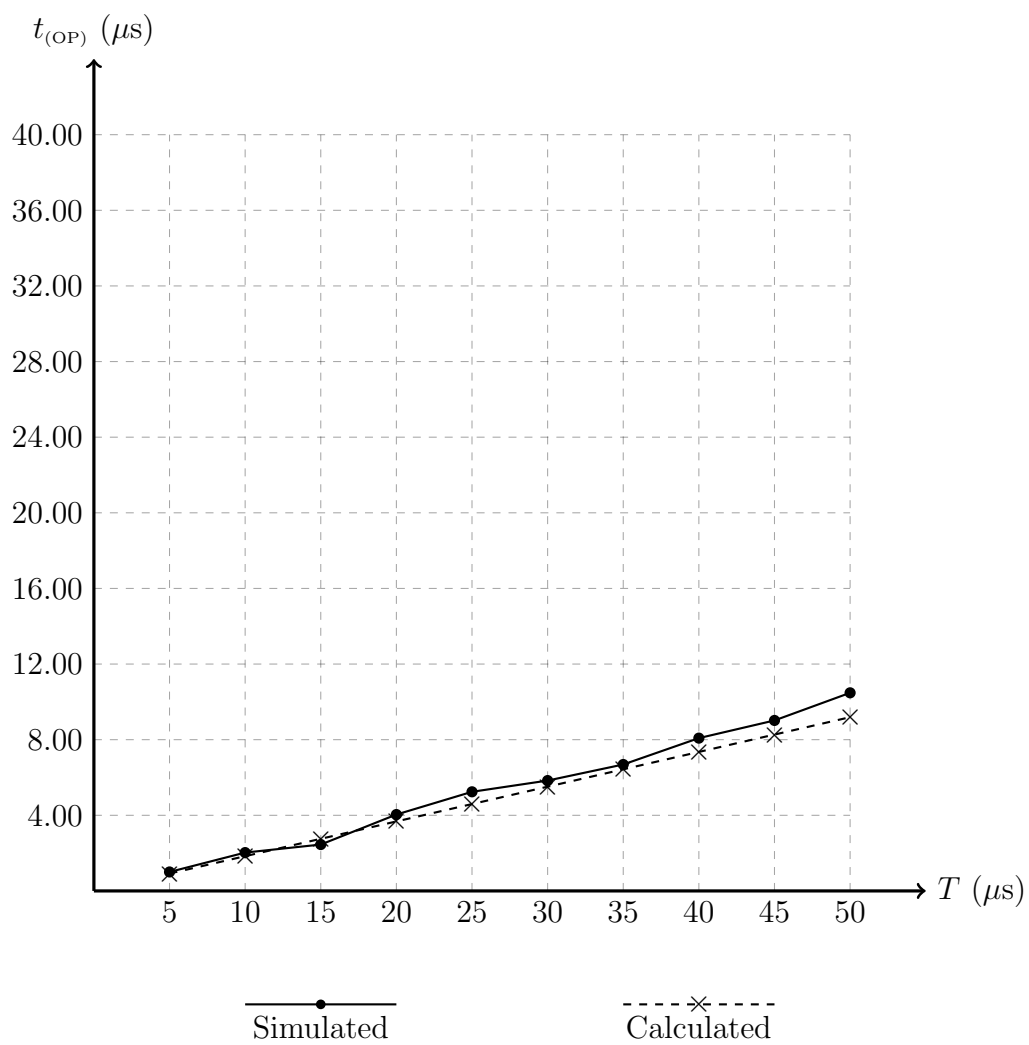


Fig. .45: Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter T from $5\mu s$ to $50\mu s$

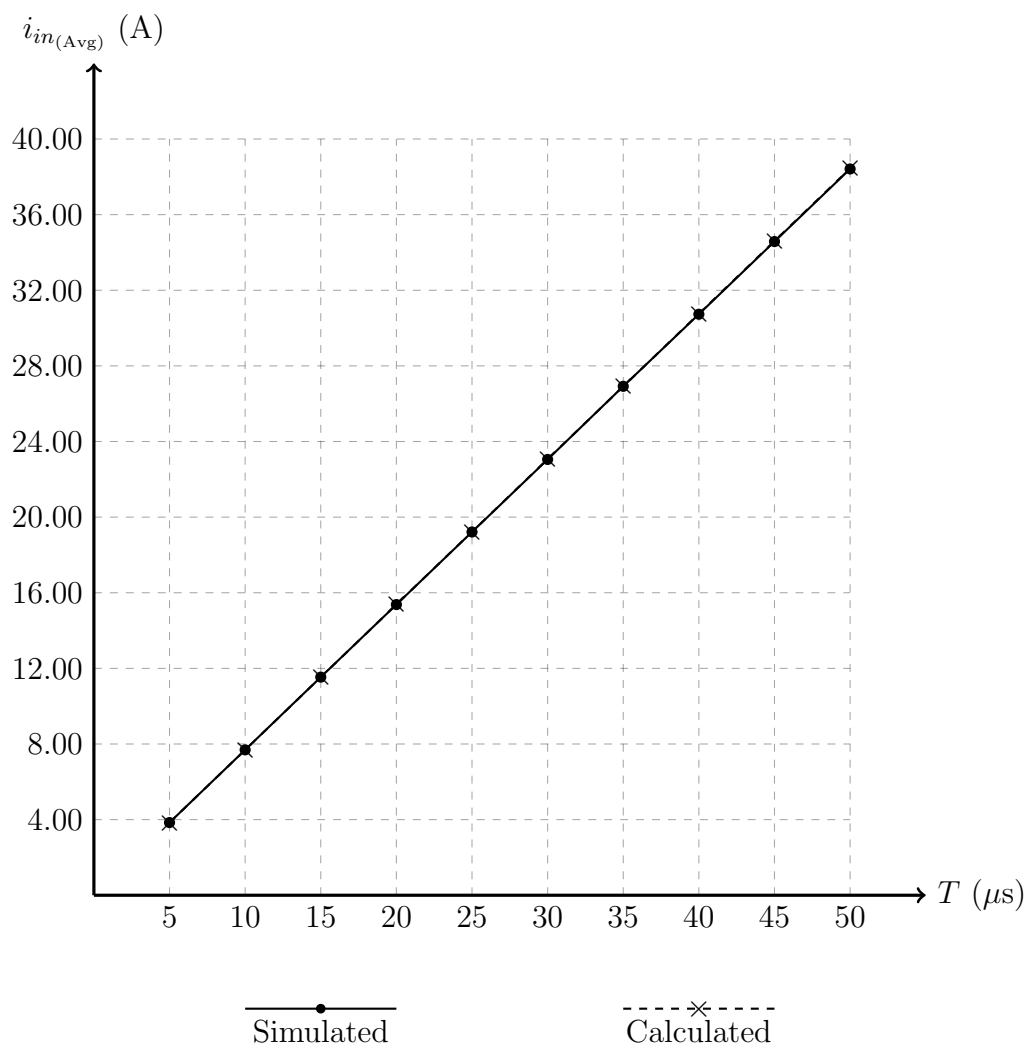


Fig. .46: Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter T from $5\mu s$ to $50\mu s$

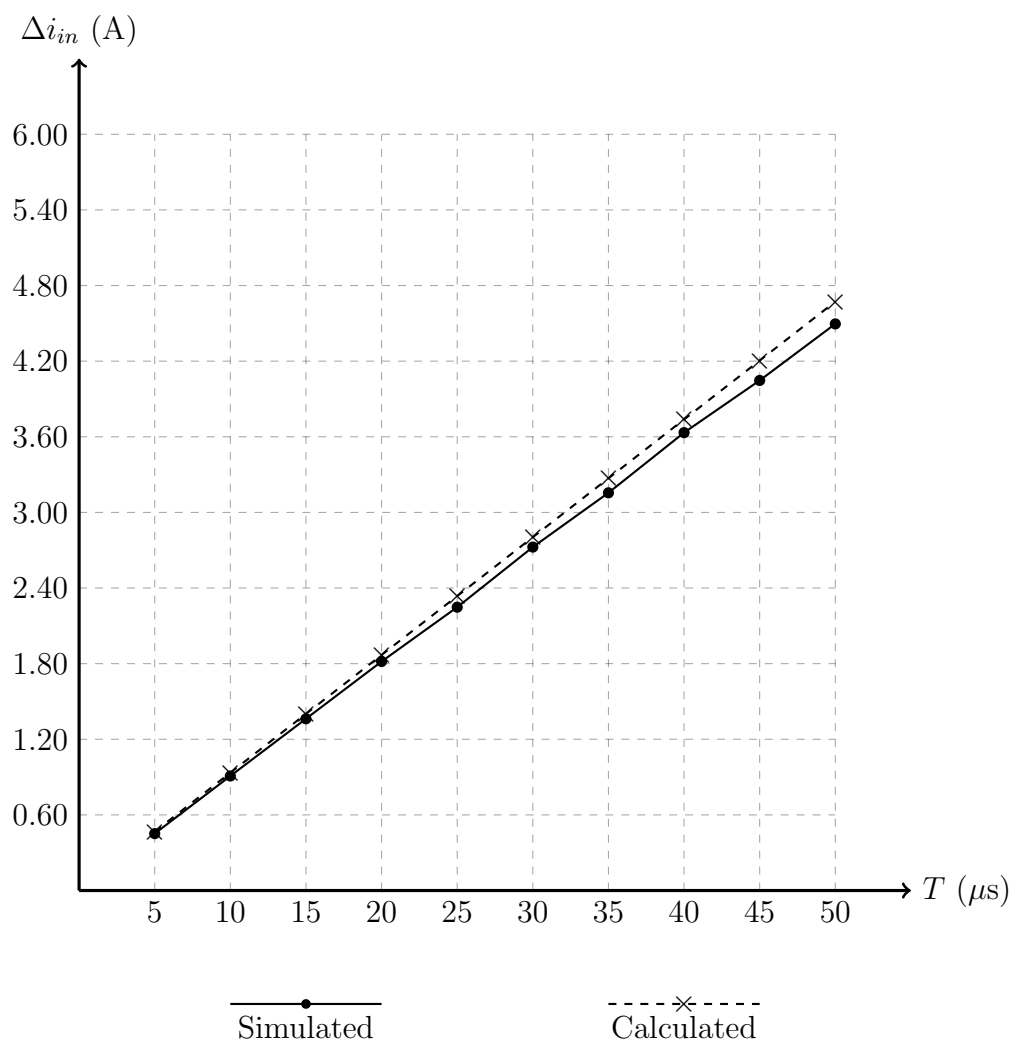


Fig. .47: Simulated vs calculated results for Δi_{in} while sweeping parameter T from $5\mu s$ to $50\mu s$

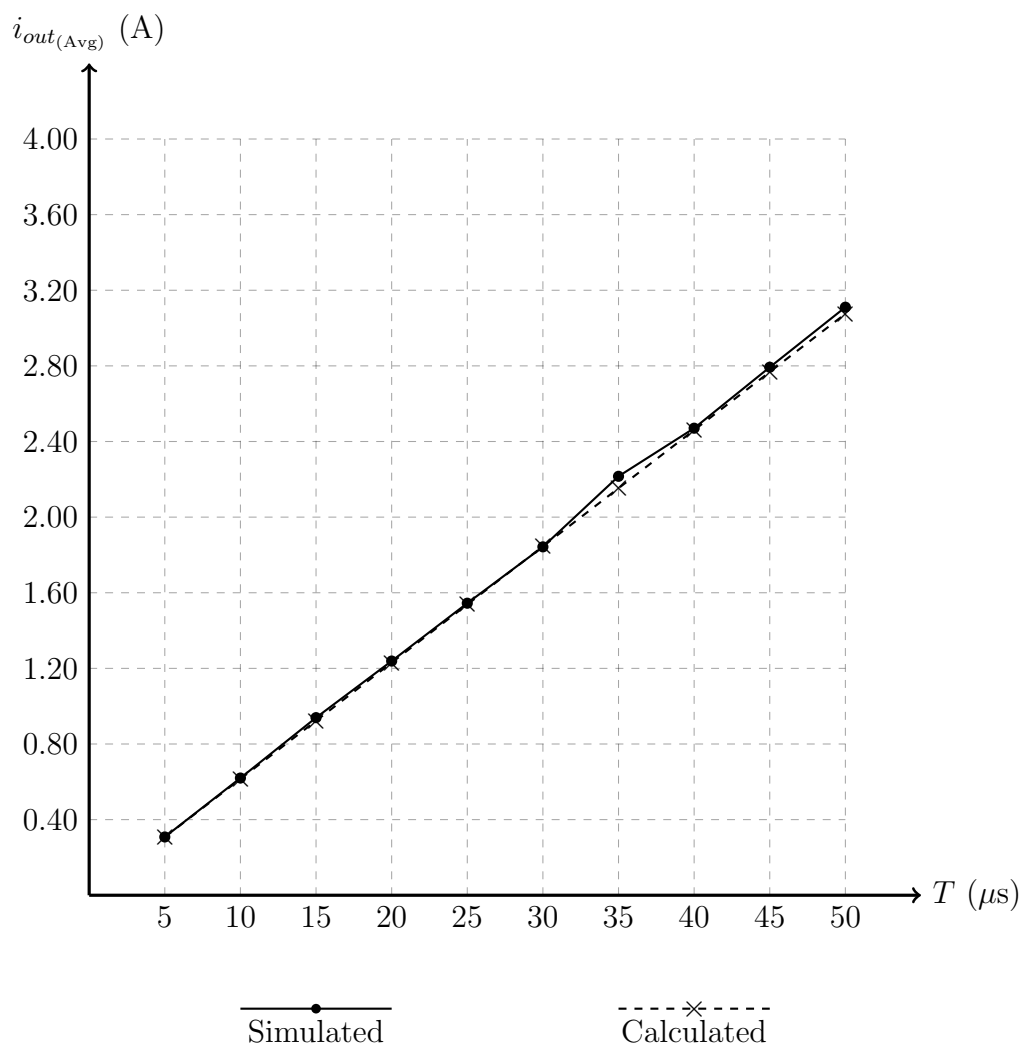


Fig. .48: Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter T from $5\mu s$ to $50\mu s$

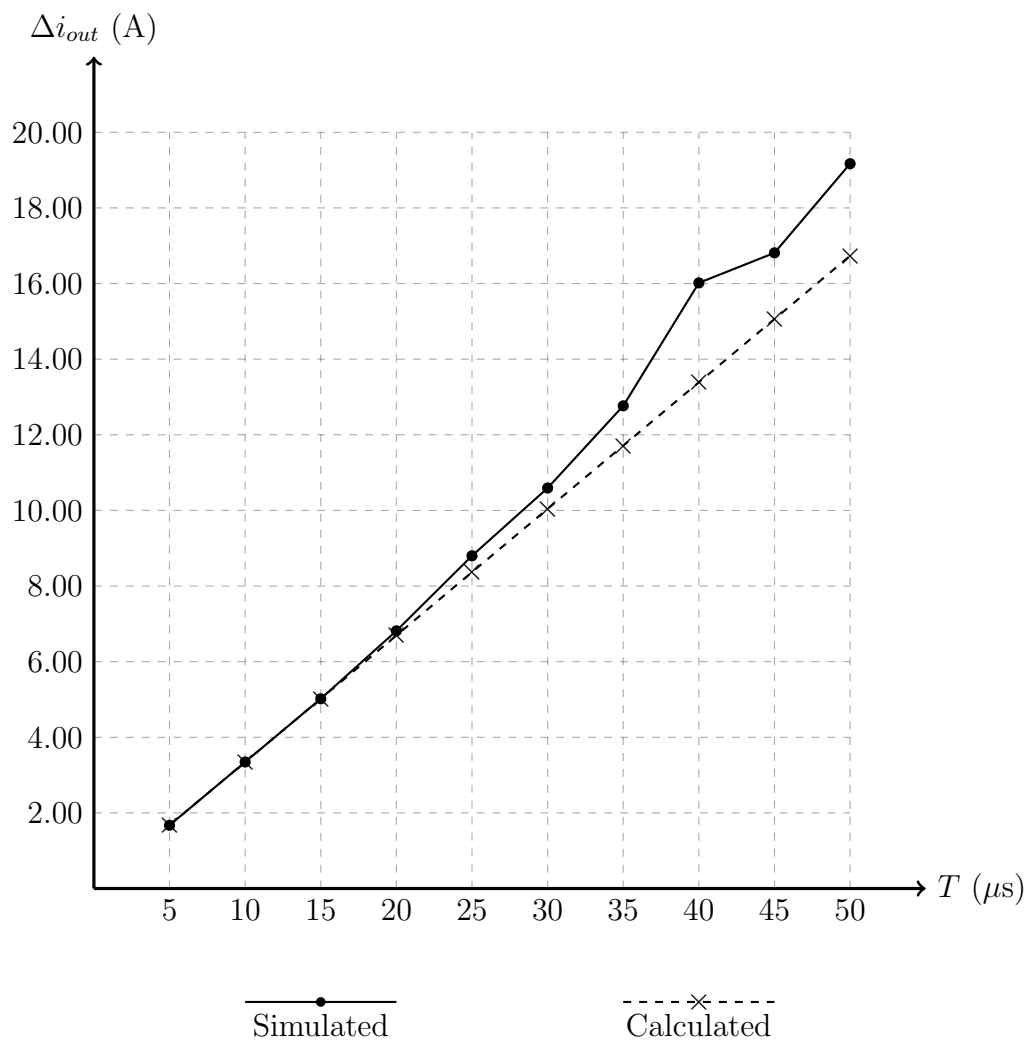


Fig. .49: Simulated vs calculated results for Δi_{out} while sweeping parameter T from $5\mu s$ to $50\mu s$

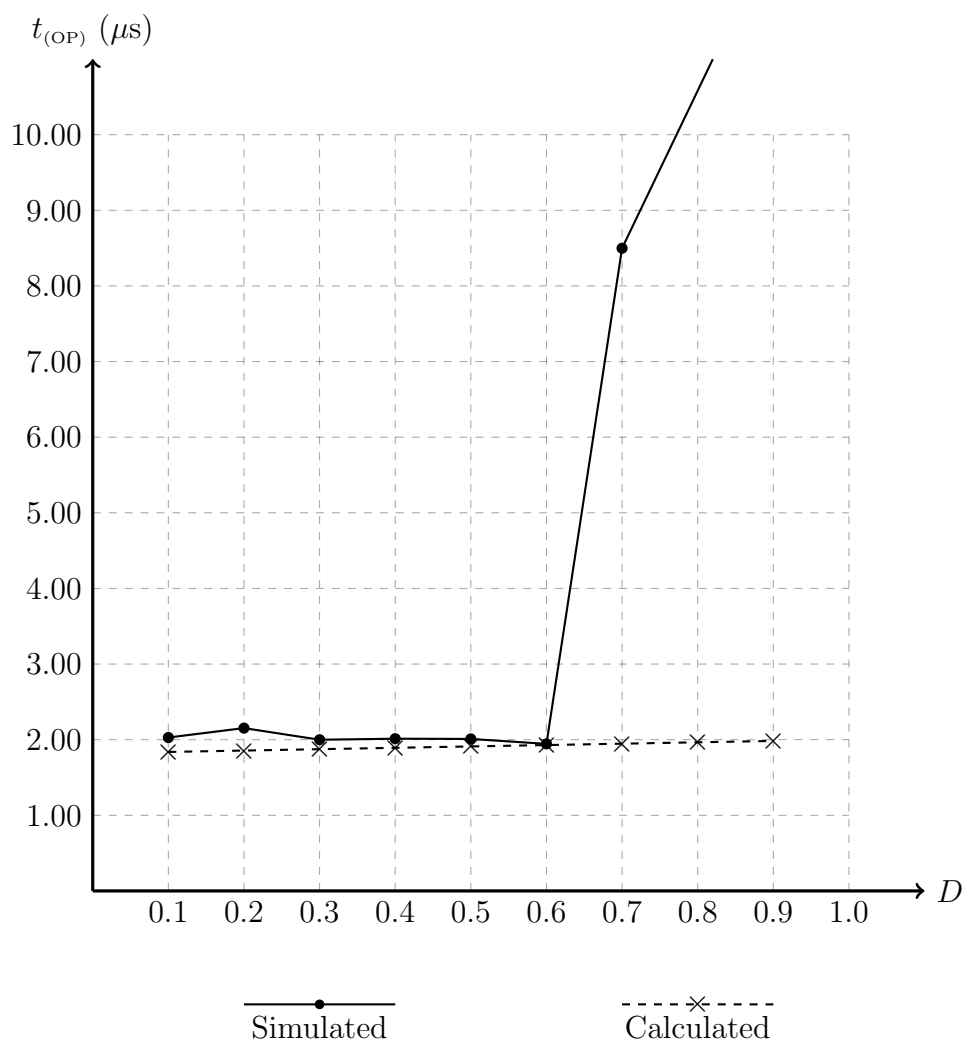


Fig. .50: Simulated vs calculated results for $t_{(OP)}$ while sweeping parameter D from 0.1 to 0.9

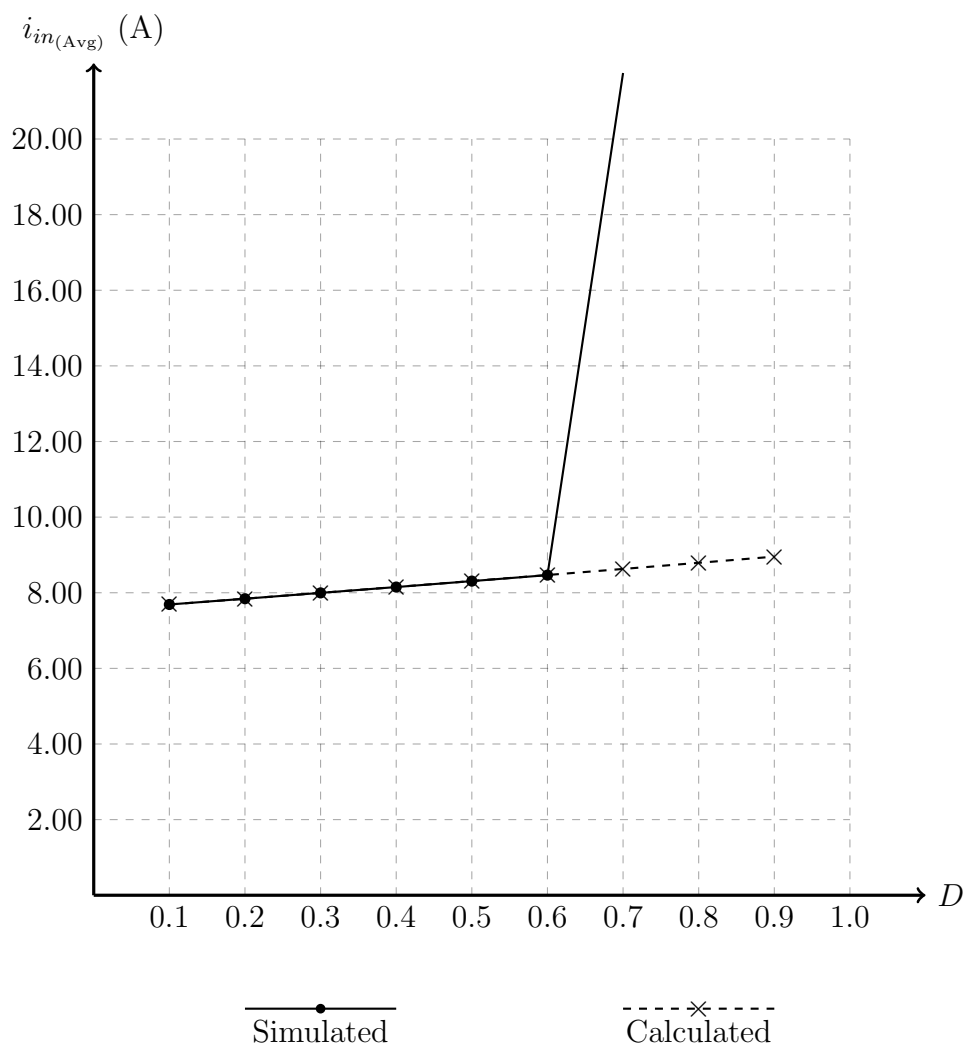


Fig. .51: Simulated vs calculated results for $i_{in(Avg)}$ while sweeping parameter D from 0.1 to 0.9

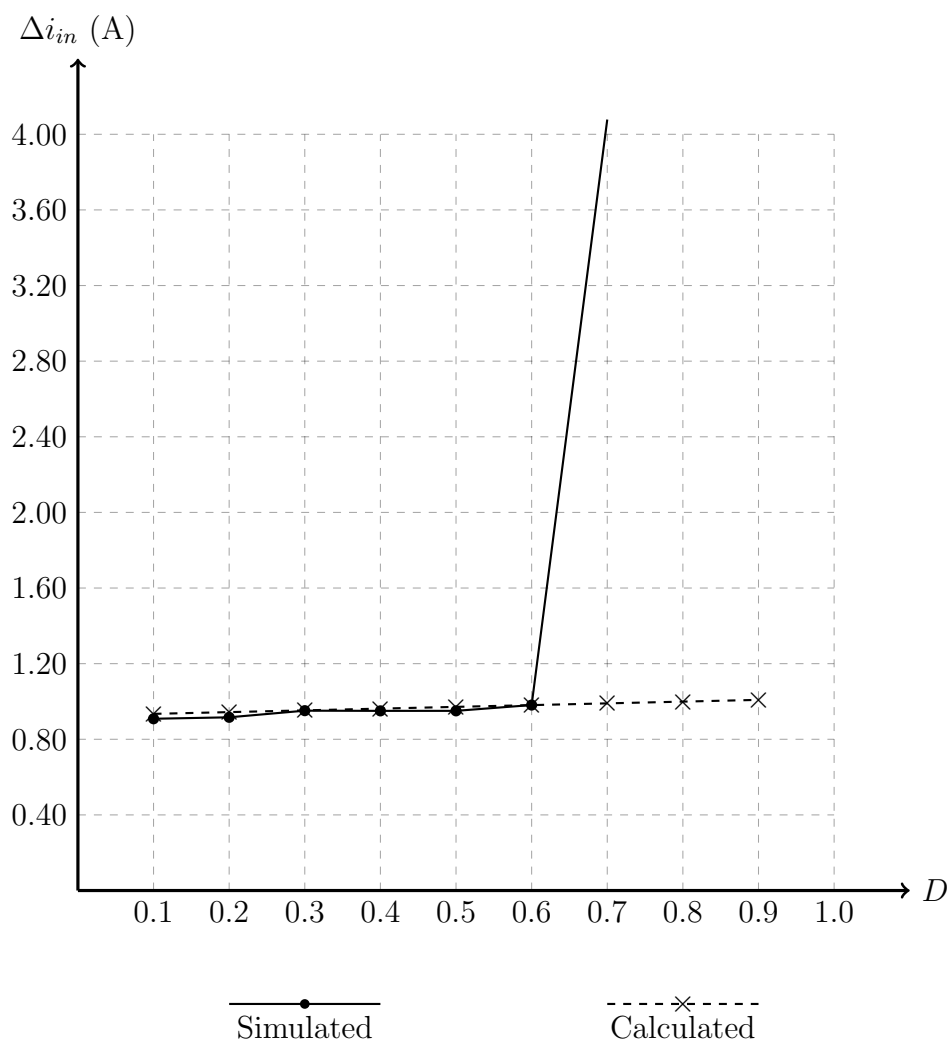


Fig. .52: Simulated vs calculated results for Δi_{in} while sweeping parameter D from 0.1 to 0.9

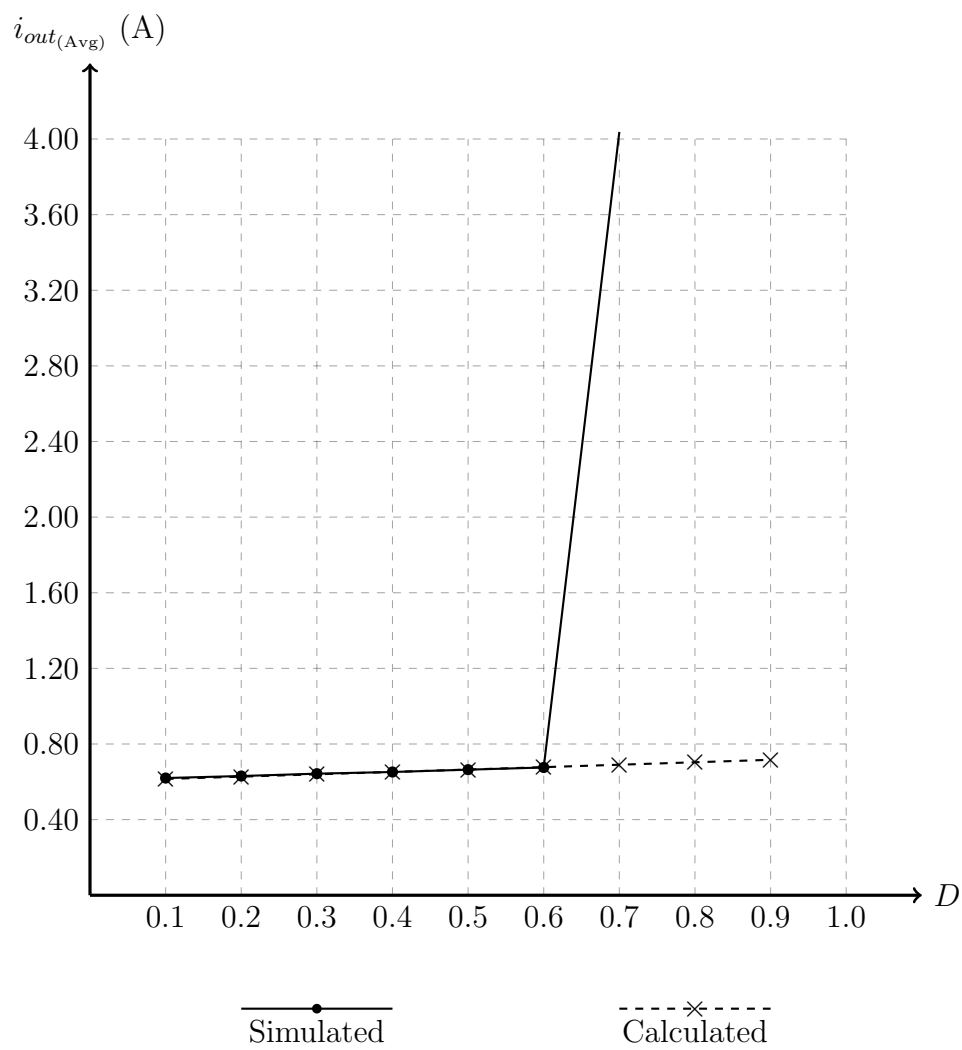


Fig. .53: Simulated vs calculated results for $i_{out(Avg)}$ while sweeping parameter D from 0.1 to 0.9

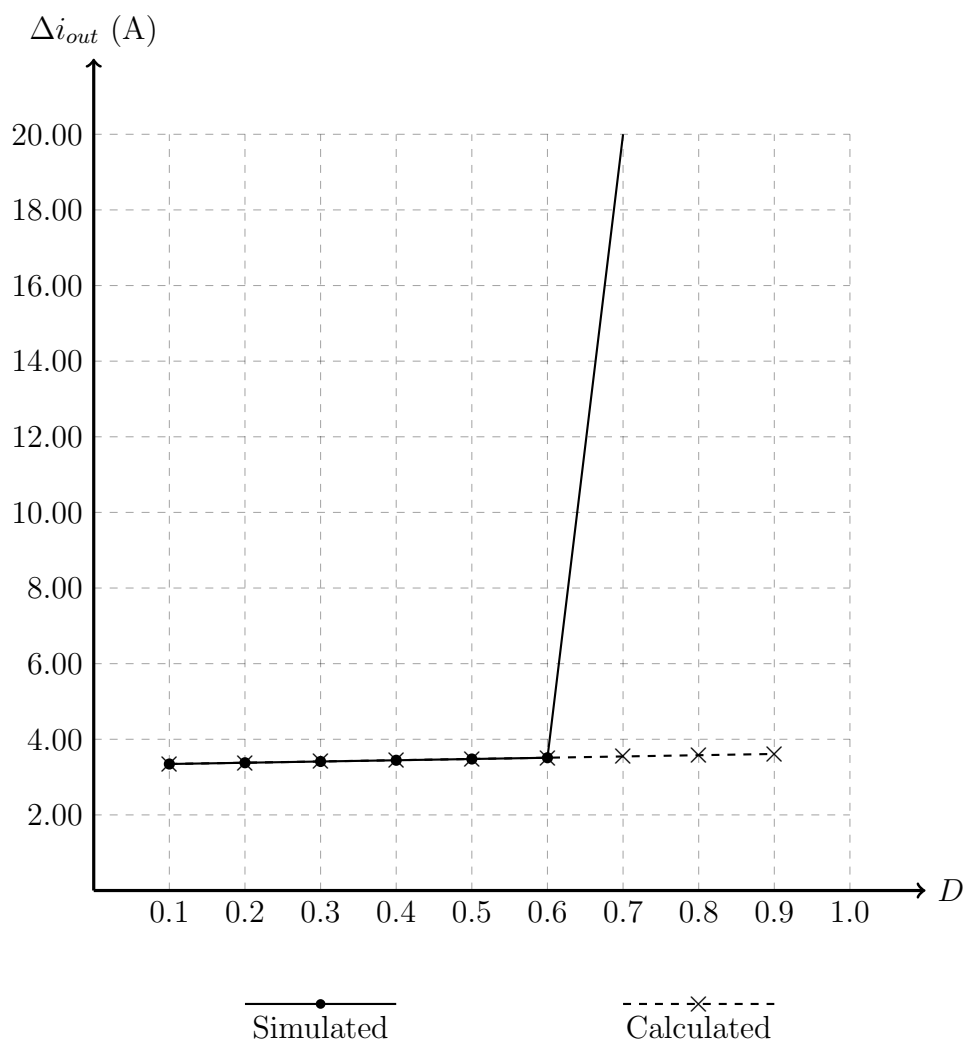


Fig. .54: Simulated vs calculated results for Δi_{out} while sweeping parameter D from 0.1 to 0.9

.8 *Non-constant output voltage prototype assembly*

This section overviews the Non-constant output voltage assembly under test in the French Riviera.

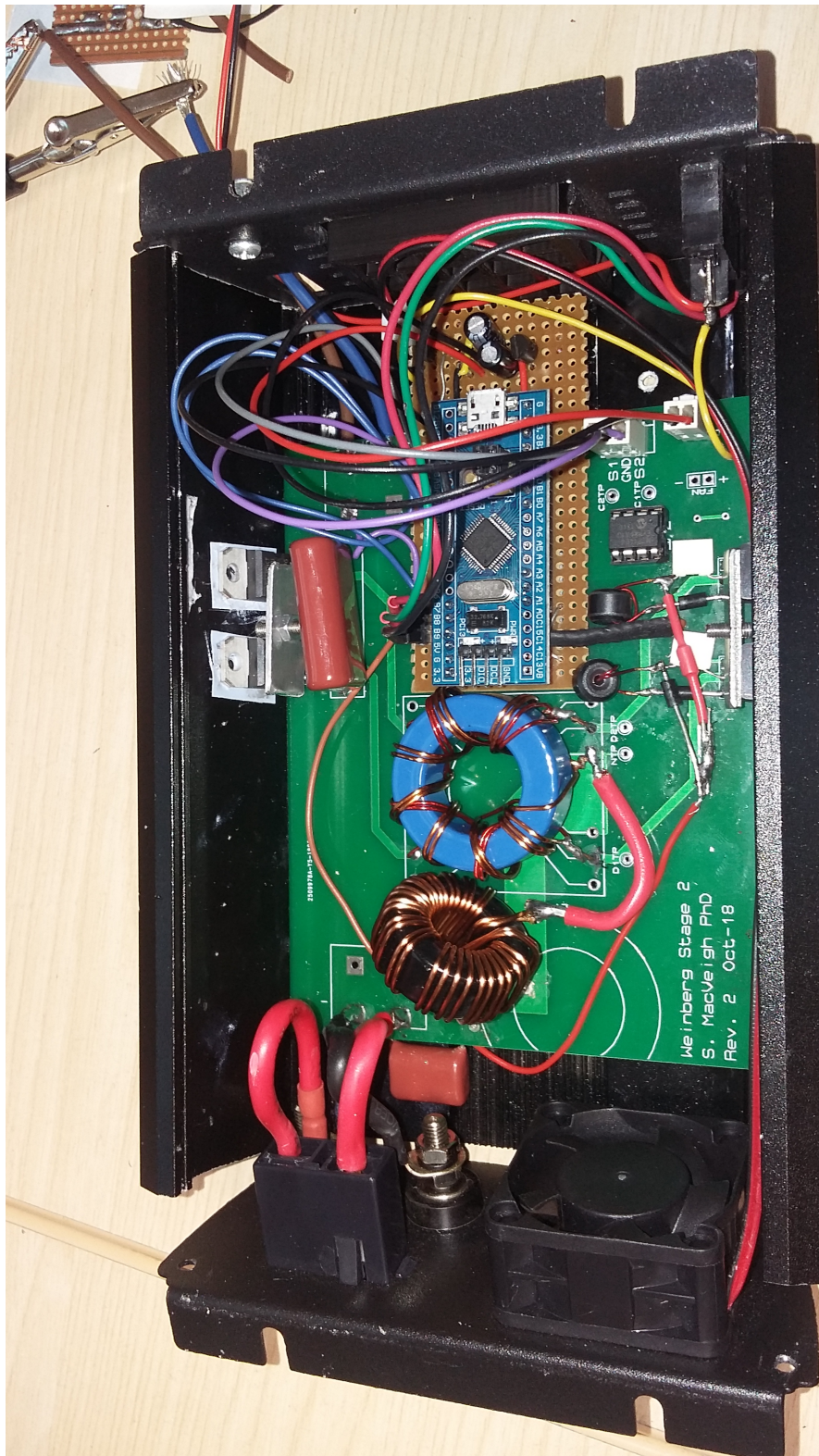


Fig. .55: Non-constant output voltage prototype assembly



Fig. .56: Non-constant output voltage prototype assembly with power measurements

Component Label (from Figure 2.1)	Value/Part
L_{A_1}/L_{A_2}	11 μ H
L_{B_1}/L_{B_2}	3.5 μ H
L_{in}	36 μ H
C_{out}	2.2 μ F 250V Film
S_1/S_2	FB260N 200V 56A Power MOSFET, $R_{DS(on)} = 40\text{m}\Omega$
D_1/D_2	STTH16R04 400V 16A Power Diode

Tab. .2: Non-constant output voltage prototype assembly component list

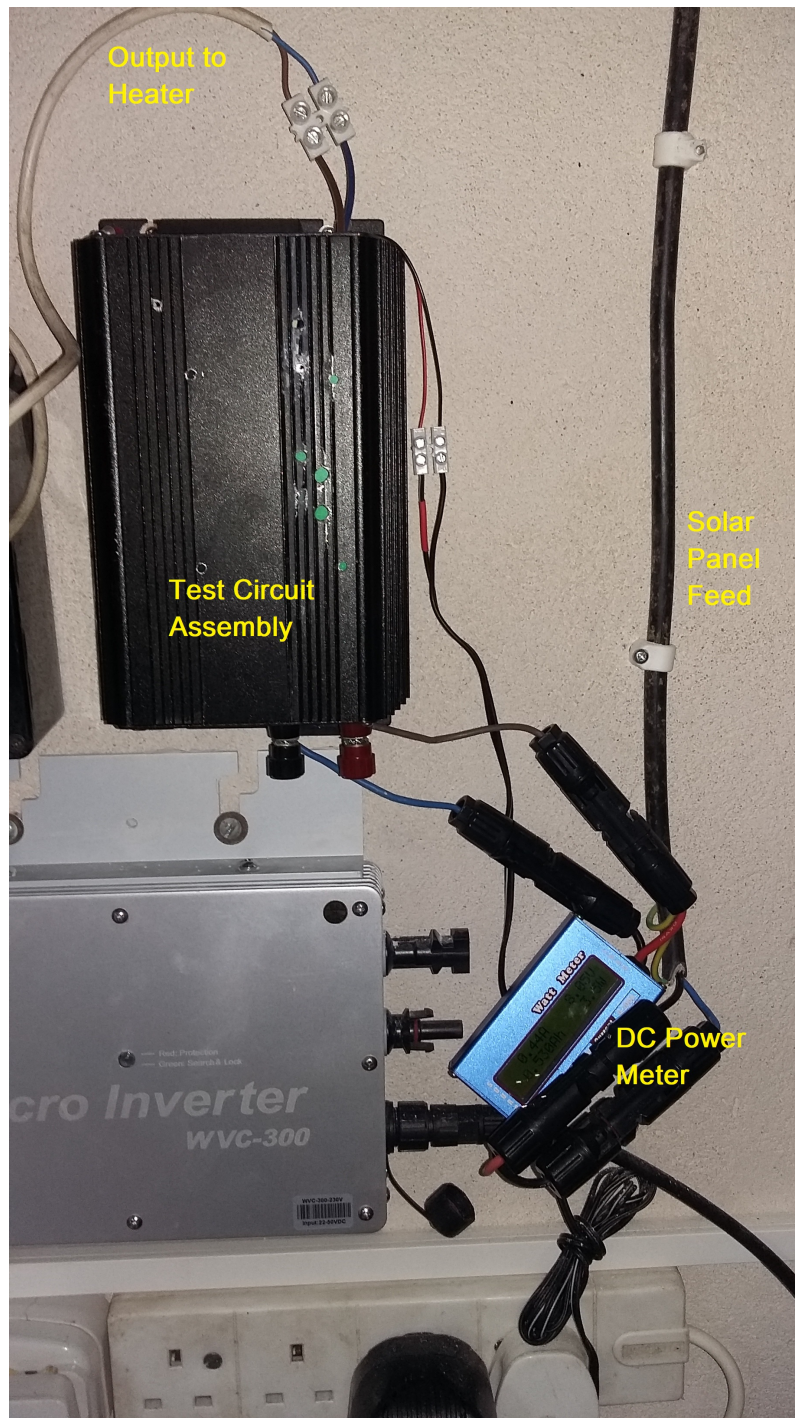


Fig. .57: Non-constant output voltage prototype assembly fitted for testing



Fig. .58: 300W solar panel in position used for testing



Fig. .59: Non-constant output voltage prototype assembly power measurements from testing